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Modeling and Simple Simulation Method of Stacked Spiral Inductors

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1. Introduction

On-Chip spiral inductors have become essential passive components for radio-frequency (RF) ICs, in which stacked inductor [1] instead of single layer can be useful because the former occupies much small chip area. The stacked inductors, however, have large parasitic capacitance compared with the single layer counterparts, resulting in lower self-resonance frequency (f_{SR}). This implies that RF-IC engineers have to pay special care for the design of stacked inductors because the self-resonance frequency f_{SR} significantly affects the characteristics of RF circuits.

In late years, several analytical models of the stacked inductor [2-3] have been reported. However, all the models reported so far are valid for only single-layer inductor so that a model for stacked inductors has been highly required to analyze the frequency characteristics of RF circuits.

The aims of this paper are twofold: (1)to introduce a simple simulation method to predict the RF characteristics of stacked inductor by using the scalable model and (2)to demonstrate the validity of the model by comparing simulated S21-parameters of two-layer inductors to the measurement ones.

2. Model and Simulation Method

Figure 1 shows a topology of stacked inductor investigated which consists of microstrip transmission lines [2]. For the analysis of the stacked inductor, a pair of adjacent single-layer lines is decomposed into short pieces of stacked transmission line with equal parasitic impedance and capacitance. This decomposition yields distributed equivalent two-port circuit model shown in Fig.2.

The frequency characteristics of the stacked inductor can be derived from distributed equivalent circuit equations, from which the two-port parameters are calculated. Figure 3 depicts the distributed circuit model at nth segment. Based on this segment model, the nodal equations is given by

$$V_{2,n+1}-(2+j\omega C_2 Z_2)V_{2,n}+V_{2,n-1}=-j\omega C_2 Z_2 V_{1,n} \quad (1)$$

$$V_{1,n+1}-\{2+j\omega(C_1+C_2)Z_1\}V_{1,n}+V_{1,n-1}=-j\omega C_2 Z_1 V_{2,n}. \quad (2)$$

where $V_{2,n}$ is the voltage at node n of upper transmission line, and $V_{1,n}$ that of bottom line. Solving the recursive equations, $V_{2,n}$ and $V_{1,n}$ can be derived as

$$V_{2,n}=\sum_{k=0}^{l}\left(\frac{C_2}{C_1+C_2}\right)^k\left\{Ae^{(n+2k)f_1}+Be^{-(n+2k)f_1}+Ce^{(n+2k+1)f_2}+De^{-(n+2k+1)f_2}\right\} \quad (3)$$

$$V_{1,n}=\sum_{k=0}^{l}\left(\frac{C_2}{C_1+C_2}\right)^k\left\{Ce^{(n+2k)f_2}+De^{-(n+2k)f_2}+\left(\frac{C_2}{C_1+C_2}\right)\left(Ae^{(n+2k+1)f_1}+Be^{-(n+2k+1)f_1}\right)\right\} \quad (4)$$

where l is a appropriate number to be converged the equations, A,B,C, and D are coefficients determined by boundary conditions, f_1 is a complex function of ω, C_2, and Z_2, and f_2 is that of ω, C_1, C_2, and Z_1. The boundary conditions are voltages at node 0 and N shown in Fig.2. These conditions are calculated by assuming that a given inductor has a linier voltage drop for the whole metal length.

In the analysis, we assumed that Z_1 and Z_2 are composed of an inductance and a resistance in series. The self-inductance of single-layer inductors was calculated based on current sheet approximation [4] and we used the same approach to calculate the mutual inductance of the stacked inductor. The resistance is computed with the analytical expression reported in [3]. The parasitic capacitances C_1 and C_2 are also calculated from the known formulation derived from classical electromagnetic theory. All these distributed circuit parameters are determined by using process data. In addition, we introduced error correction parameters extracted from experimental data in such a way that calculation results fit with measured data. The correction parameters depend on a process technology but not vary significantly in the same technology. With this approach, Y-parameters can be calculated and we obtain S21-parameters by using

$$S_{21} = \frac{-2Y_{21}}{(1+Y_{11})(1+Y_{22}) - Y_{12}Y_{21}} \tag{5}$$

where Y-parameters are normalized for a characteristic impedance of a transmission line in a measurement system.

3. Results and Discussion

The experimental S-parameter data were collected from on-wafer measurements. The test structure used was a square, stacked spiral, five-turn inductors fabricated with 0.20 μm SOI-CMOS technology with four metal layers (M_4 ~ M_1). We designed the inductors with M_3 and M_2, M_4 and M_3, or M_4 and M_2 to investigate the effect of parasitic capacitances coupling inter-metal layers and bottom-layer on the shift of f_{SR}.

Figure 4 (a), (b), and (c) reveal that the interlayer capacitances are dominant on the f_{SR} shift. The stacked inductor with M_4 and M_2 has higher f_{SR} because the interlayer capacitance C_2 is smaller than others. These results demonstrate that a higher f_{SR} is achieved to separate the single-layer inductors of stacked structure from each other.

Figure 4 (a)-(c) show that the measured data are compared with the simulation results. They are simulated with the use of the correction parameters extracted from the data of the inductor composed of M_3 and M_2. Note that the simulation results of the S_{21}-parameter agree well with measured results over all frequency range.

4. Conclusion

We proposed a simple numerical method using a scalable distributed circuit model to predict the frequency characteristics of a stacked inductor. The comparison of the measured and simulated results demonstrated that the proposed two-port model is valid and useful for the analysis of a stacked spiral inductor.

Acknowledgment

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References

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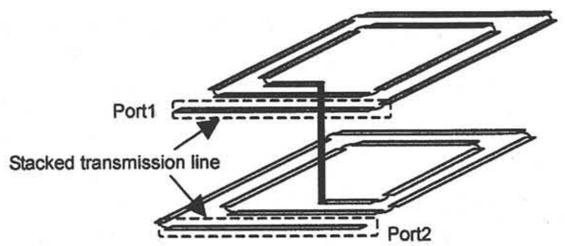

Fig.1 Two-layer stacked spiral inductor

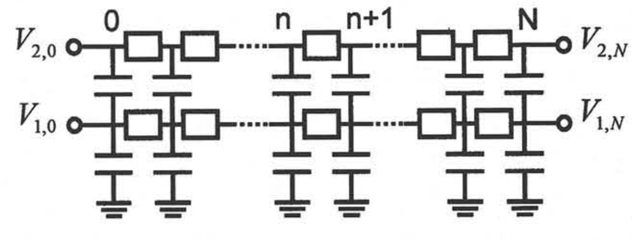

Fig.2 Distributed two-port equivalent circuit model

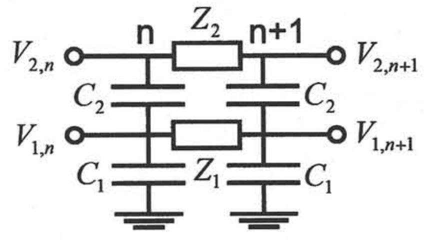

Fig.3 nth segment of distributed circuit model

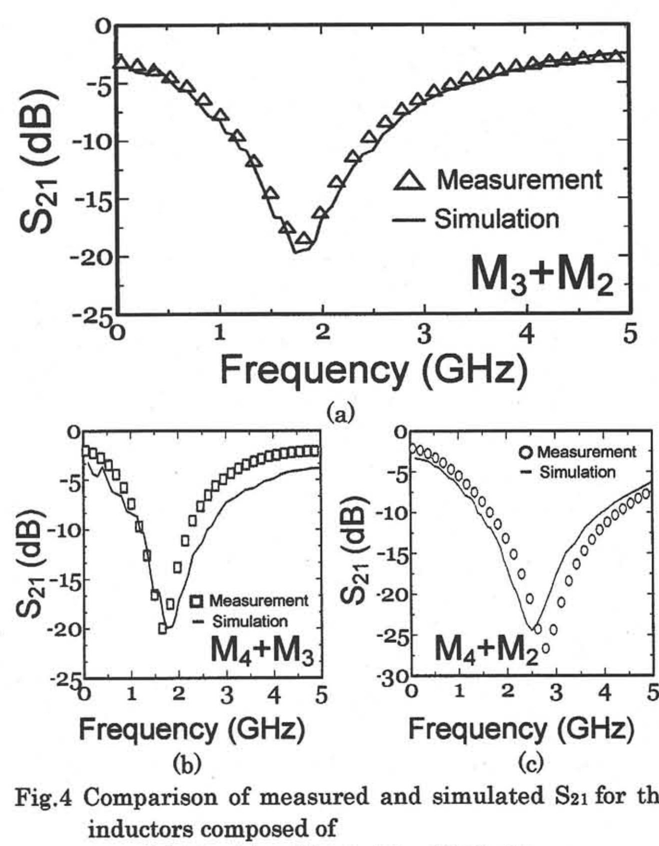

Fig.4 Comparison of measured and simulated S_{21} for the inductors composed of
(a) M_3 +M_2 (b) M_4+M_3 (c) M_4+M_2