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Ultra-thin Silicon Channel Single- and Double-gate MOSFETs

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1. Introduction

To achieve higher performance, lower power, and higher integration density, the reduction of feature sizes for semiconductor devices will continue following Moore's law. Fig. 1 shows the gate length and equivalent gate oxide thickness needed in each technology node based on the 2001 ITRS. High-k gate dielectric and metal-gate will be needed to meet the EOT requirement. Extremely shallow and abrupt junctions with high dopant activations are vital to control short-channel effect and to give high drive-current. This will require zero thermal cycle and super-activation for junctions engineering. Line-edge roughness in small transistors increases the leakage current and potentially limits the scaling of transistors. Alternative gate patterning and etching process will be needed. Conventional CMOS scaling has become extremely difficult. SOI technology offers performance enhancement over bulk CMOS because of junction capacitance reduction and lack of body effect. Scaling barrier could be overcome if the silicon channel of is scaled to ultra-thin regime. This paper will discuss recent progress and challenges of ultra-thin silicon channel single- and double-gate FET.

2. Ultra-thin Silicon Channel SOI MOSFET

Many researchers have analyzed the scaling characteristics of ultra-thin body SOI FETs. [1-4]. An extremely thin (< 10nm) silicon channel is required in order to support the gate length scaling for sub-25 nm devices and below. The double-gate FET has a 2X reduction in depletion-width and the drain to body fringing field through the BOX is substantially less. Numerical simulations show a 2.5X to 3X better scalability (Figure 2). The major challenges associated with ultra-thin channel are: 1) SOI thickness variations, 2) high series resistance, 3) multiple-threshold voltage setting, and 4) carrier transport not understood.

Figure 3 shows a cross-section of an ultra-thin silicon channel FET with 3.7nm SOI thickness. A raised source/drain process reduces the external resistance. The use of halo and channel doping are the standard and most effective way to implement multiple-threshold voltages in conventional CMOS. However, dopant fluctuation effect will surely become problematic in such small dimensions. Gate workfunction engineering is likely needed for threshold voltage setting. While some theoretical studies predicted enhanced mobility in ultra-thin silicon-channel MOSFETs, experimental data indicates mobility degradation may be a problem (Figure 4) [5,6].

3. double-gate SOI MOSFETs

We have fabricated high-performance double-gate devices in both planar and FinFET structures. The performance of these devices can rival conventional CMOS devices. Figure 5 shows a cross section of a planar double-gate device [7]. Because the DG is operating at a much lower effective field the mobility of the DG could be two times higher compared to that of the scaled bulk CMOS at the operating condition (see Fig. 6). Under single-gate operation, the front-gate threshold voltage can be modulated by the back-gate bias, providing opportunity for leakage reduction and performance enhancement. However, the trans-conductance is also affected by the back-gate (Fig. 7). These devices can also be used to study the characteristics of symmetric-double-gate (SDG), asymmetric double-gate, and single-gate MOSFETs. In any double-gate structures, the top and bottom gates must be self-aligned to each other in order to reduce series resistance and overlap capacitance. The fabrication process to meet such requirement in a planar structure is extremely difficult. The FinFET structure is self-aligned and has been described as the easiest to fabricate [4,9]. A cross-section of a FinFET is shown in Fig. 8 [8]. Record high double-gate current was enabled by selective-epitaxial process to expand the source/drain regions (Fig. 9). The major disadvantage of the FinFET structure is that the most critical dimension, channel thickness, is controlled by lithography and etching. The side-wall-image transfer process has recently been shown to be capable of generating very small line widths with small variations [9].

4. Conclusions

The scaling issues of ultra-thin silicon channel MOSFETs have been examined. Tremendous progresses have been made in fabricating ultra-thin silicon channel single-gate and various double-gate devices. While the scalability is promising, solutions for gate workfunction engineering and channel thickness control are critical for these devices to be competitive to replace conventional CMOS device structures.

Acknowledgments

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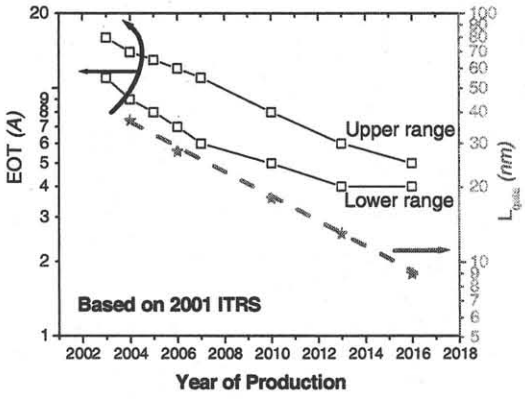

Fig 1: Technology Scaling.

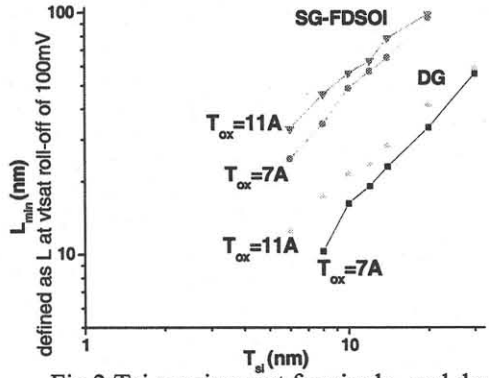

Fig 2:Tsi requirement for single- and double-gate MOSFET to support gate length scaling.

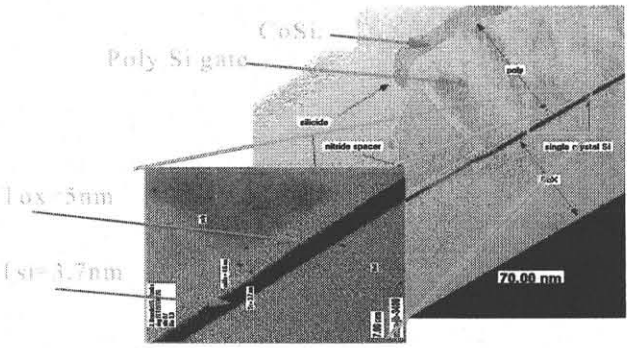

Fig 3: Cross-section and TEM of an ultra-thin silicon channel single-gate MOSFET.

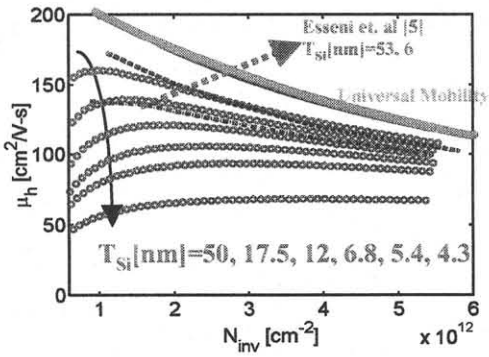

Fig 4: Effective hole mobility as function of SOI thickness and inversion charge density.

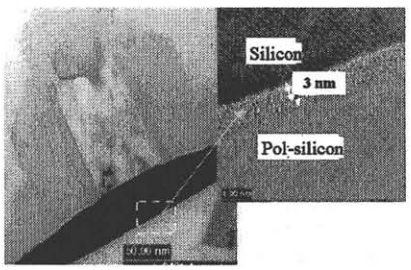

Fig 5: Cross-section of a high-performance planar double-gate MOSFET with 3 nm back-gate.

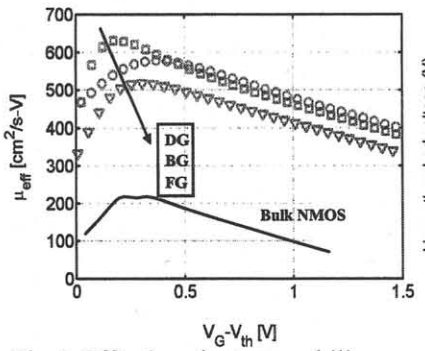

Fig 6: Effective electron mobility as a function of gate over-drive.

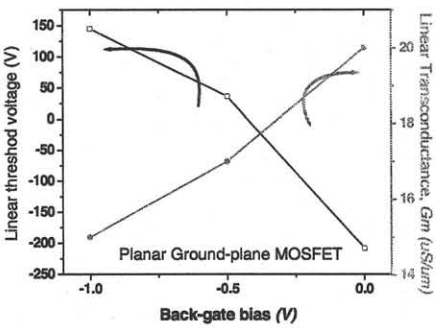

Fig 7: Vt and Gmlin vs. back-gate bias.

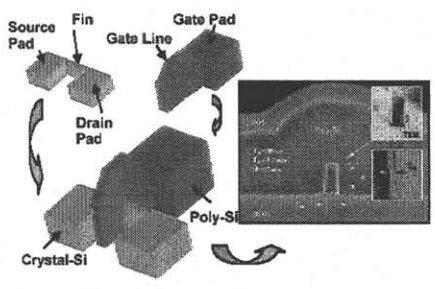

Fig 8: Cross-section normal to the current carrying plane of a high-performance double-gate FinFET

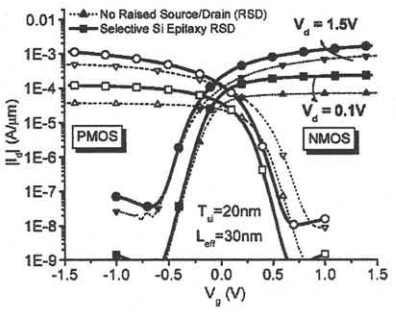

Fig 9: Ids-Vgs characteristics of double-gate FinFET.

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