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Corrugated-Channel Transistor (CCT) for Area-Conscious Applications

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1. Introduction

To achieve higher performance of MOS FET, V-shaped FET [1] and vertical channel FET [2] were proposed in early 1970's however, the device scaling in planar area has only been a long lasting trend up to date except a case of trench-capacitor DRAM which has already incorporated etched trench, formed into silicon substrate [3], in it. Extending this trend, DELTA [4] and fin FET [5] have recently been proposed.

In this presentation, a 3-D transistor with relatively tall multifins is proposed. This is named CCT (Corrugated-Channel Transistor) after its "corrugated structure" which is formed vertically into {110} silicon substrate by TMAH (Tetra methyl ammonium hydroxide); it has been widely used as a photoresist developer. Etched cross sections are shown in Fig. 1.

The basic concept of CCT with increased effective-channel width is shown in Fig. 2. Device performance of this CCT structure is demonstrated hereafter.

2. Fabrication Processes

An orientation-anisotropic etching with TMAH is a key process to achieve truly vertical channels in terms of orientation selectivity. Obtained etch rates are shown below with 2.5-% TMAH aqueous solution at 75°C.

Material	Etch rate	Relative to {111}
{110} Si	606 nm/min	132
{111} Si	4.6 nm/min	1
SiO ₂	0.8 nm/min	0.2

Thus, the selectivity of {110} to {111} exceeds 130. Even if the selectivity is big enough in this case, it rapidly gets worse with the increase in angle deviation of mask edge from the exact [112] direction. Precise control of mask-edge direction is inevitable for good reproducibility. Obtained structure is shown in Fig. 3 with channel width of 54 nm. Even 24-nm thick and 900-nm tall beams were successfully delineated with the TMAH etching. Its aspect ratio is almost 40.

Since oxidation rates differ in crystal orientation, 14.2-nm and 13.4-nm thick oxides are formed on $\{110\}$ and $\{111\}$ surfaces, respectively, with 1000°C dry oxidation. Protruding edges are formed in principle resulting in thinner SiO₂ at the edges as shown in Fig. 4.

3. Device Characteristics

All devices were fabricated on {110} substrate of 80- Ω -cm resistivity ($N_A = 2 \times 10^{14}$ cm⁻³) with no channel implantation in order to enhance depletion phenomena of the corrugated channels. Thus, threshold voltages of one-beam CCT, as shown in Fig. 5, are all negative. In addition, threshold voltage swings are shown in Fig. 6 for one-beam CCT indicating that the swing

change saturates at beam thickness below $0.96 \,\mu\text{m}$. This is because the beam is completely depleted resulting in no additional change in threshold voltage swing. Their *C-V* characteristics of MOS capacitors show the same tendency.

Typical I_d - V_d characteristics of a CCT with 31 beams are shown in Fig. 7 without distinguishable problem. As a series resistance of source and drain is estimated to be less than 20 Ω causing no adverse effect.

Transconductance, G_m vs. applied gate voltage is shown in Fig. 8 with a parameter of number of beams. In addition, as $G_m max$ is observed to be accurately proportional to the total effective channel width, electric field concentration effect caused by edge SiO₂ thinning, previously shown in Fig. 4, can not be analytically separated.

To summarize the device performance, drivability of CCT is shown in Fig. 9. It is obvious that CCT achieves almost 5 times bigger drivability than that of planar at the same planar area of $100 \,\mu\text{m}^2$. When the beam density becomes higher, its commensurate device performance can be expected.

4. Conclusion

A novel 3-D MOS transistor, named CCT (Corrugated-Channel Transistor), with $1-\mu m$ tall and 54-nm thick multibeams has been realized utilizing crystal orientation anisotropic TMAH etchant on {110} silicon substrate. Any degradation has not been observed yet in device performance due to beam edges. With the increase in number of beams, drivability increases almost proportional to that number. As a consequence, it is clarified that planar area-conscious applications are feasible with the use of CCT.

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Fig. 1 SEM micrographs of etched grooves formed on {100} (a) and {110} (b) silicon substrates with 2.5% TMAH etchant at 75°C.



Fig. 2 A basic structure of CCT (Corrugated-Channel Transistor) and its effective-channel width increase with number of beams. Total effectve gate width, $W_{g,l} = 2W_{pl} + 2W_{p2} + 3T_B + 6H_B$, Projected planar gate width, $W_{g,p} = 2W_{pl} + 2W_{p2} + 3T_B$, thus, $W_{g,l} = W_{g,p} + 6H_B$.



Fig. 3 Corrugated channels covered by polysilicon gate consist of 24 beams of 54 nm in thickness and 900 nm in height.



(a) Top edge of a beam (b) Bottom edge of a beam

Fig. 4 TEM micrographs showing conformability of SiO_2 formed by dry oxidation at 1000°C at top (a) and bottom (b) edges of a beam.



Fig. 5 Threshold voltages of one-beam CCT as comapred to that of planar transistor.



Fig. 6 Threshold voltage swing, ΔV_{th} vs. substrate bias. The swing variation saturates at the beam thickenss below 0.96 μ m.



Fig. 7 Typical I_d - V_d characteristics for a CCT with 31 beams of 54-nm in thickness and 900 nm in height.



Fig. 8 Transconductance, G_m vs. gate voltage with a parameter of number of beams.



Fig. 9 Drivability increase with number of beam increasing.