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An Electrostatic-Discharge(ESD) Protection Device with Low Parasitic Capacitance Utilizing a Depletion-Layer-Extended Transistor(DET) for RF-CMOS IC's

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Abstract

In this paper, an Electrostatic-discharge(ESD) protection device for RF-CMOS IC's utilizing the Depletion-layer-Extended Transistor(DET)[1] is reported. The DET, which reduces the area-component of junction capacitance by about 1/3, realizes an ESD protection device with low parasitic capacitance. With Transmission Line Pulse(TLP) testing, the DET demonstrates about the same or higher ESD robustness as compared with the conventional. The junction capacitance of the proposed device to obtain a failure current(It2) of 1-1.33A in TLP testing corresponding to a Human Body Model(HBM) tolerance of 2kV is estimated to be very low, less than 150fF.

1. Introduction

A grounded-gate NMOS(ggNMOS) device(Fig.1(a)) is widely used as a reliable ESD protection device in CMOS IC's. It is well known[2-4] that drain-contact to gate spacing(DCG) has to be enlarged to 2-5μm with the silicide block process, to obtain a sufficient and stable ESD robustness in this device(Fig.1(b)). Therefore, the ggNMOS results in extremely large parasitic capacitance with junction capacitance(C_j), as shown in Fig.1(c). This raises serious problems in RF-CMOS IC's[5-6] now being developed, which demand low parasitic capacitance to prevent significant RF-signal-loss and noise-increase[7-8]. Recently, the DET has been proposed for the RF switch circuit in a CMOS process, which realizes a low insertion-loss with significant C_j reduction and substrate resistance increase[1]. In this paper, to realize a low parasitic capacitance ESD protection device suitable for RF-CMOS IC's, we apply the DET to the ggNMOS and demonstrate its ESD protection characteristics.

2. Application of DET to ggNMOS ESD protection device

The NMOS transistor(Tr) called DET has been proposed[1], where ion-implantations(I/Is) of punch-through stopper(PTS), p^+isolation and p-well are omitted with the intention of reducing C_j by enlargement of the source/drain(S/D) depletion-layer-width(Fig.2). Although these three I/Is are generally indispensable in a CMOS process, we intentionally do not implant them for the DETs utilized only in the regions of ESD protection devices against RF input/output pads. A very shallow channel doping(CD) for V_t-control and a p^+pocket structure are commonly applied to the DET and conventional Tr. Since both types of Trs are simultaneously formed with the addition of only one mask-step to the standard CMOS process, process-cost increase can be minimized. Figure 3 shows net-impurity-concentration vertical-profiles at the center of the S/D region for both types of Trs by a two-dimensional(2D) process-simulation. The p-type impurity concentration of the DET below the junction is remarkably reduced to a very low quantity of less than $10^{16}cm^{-3}$. Figure 4 shows device-simulation results of electric field strength in the non-bias condition. Considering a depletion-layer as a region where high electric field strength exists, the junction depletion-layer in the DET is dramatically extended only in the vertical direction as compared with the conventional Tr. In an actual 0.18μm-rule fabrication, the DET successfully reduces the area-component of C_j by about 1/3, as shown in Fig.5. Figure 6 shows L dependence on off-leakage current characteristics. Although off-leakage current of the DET is increased by about two orders, L dependence on its off-leakage current characteristics is very stable. With its use of the limited number of Trs, there is no problem for off-leakage current characteristics. Here, one might be concerned that the omission of the p^+isolation I/I could cause an isolation problem. However, we apply the DET only to the limited number of Trs and the isolation width in these regions can be ensured to be sufficiently wide to avoid the isolation problem.

In the ggNMOS, the area-component occupies more than 90% of C_j because of the large DCG. Therefore, the 1/3 reduction of the C_j area-component with the DET contributes to almost a 1/3 reduction of C_j in the ggNMOS. If the DET maintains at least the same ESD tolerance as compared with the conventional, the DET realizes a low parasitic capacitance ESD protection device.

3. TLP characteristics of ggNMOS utilizing DET

The TLP testing[9] of ggNMOS ESD protection devices utilizing the DETs has been performed. The TLP testing is well known as a useful method to measure I-V characteristics during an ESD protection operation of the device and predict its ESD robustness[10-11]. Figure 7(a) shows TLP characteristics of the DET as compared with the conventional Tr. Here, DCG was 4μm. As a first trial, L was set to be 0.5μm, which was not the optimized value. The failure current, It2, of the DET was found to be about the same or higher than the conventional. Furthermore, as can be seen in Fig.7(b), which is the magnified figure of the snapback region of Fig.7(a), the trigger voltage(Vt1) of the DET is reduced by about 1V as compared with the conventional. Here, it is well known that the condition of Vt1<Vt2, the so-called 'uniformity condition', has to be satisfied to obtain uniform triggering in a multi-finger ggNMOS, which is indispensable to a reliable and stable ESD protection operation[12,4]. To satisfy this condition, the enlargement of DCG to 2-5μm to increase Vt2 has been adopted. Therefore, the Vt1 reduction with the DET contributes to reduction of DCG and C_j. The parasitic bipolar action of the ggNMOS during ESD stress is explained in Fig.8. It can be seen that the trigger voltage of the bipolar action, that is, Vt1, is reduced by the DET, owing to the effect of increase of R_{sub} in Fig.8. Figure 9 shows DCG dependence of TLP characteristics of the DET. Even the case of DCG=2μm is sufficient to satisfy the uniformity condition of Vt1<Vt2. This result shows that further DCG reduction to less than 2μm will be acceptable. From the previous investigations [10-11,13] of the correlation between TLP and HBM, an It2 of 1-1.33A has to be accomplished in TLP to ensure an HBM robustness of 2kV. In the proposed DET, this It2 value can be realized with W<150μm and DCG<2μm. At this time, its C_j can be estimated to be less than 150fF. Finally, s-parameter characteristics in the RF range from 0.1 to 6GHz were investigated(Fig.10), and the results support successful reduction of parasitic capacitance of the ggNMOS by the DET.

4. Conclusion

A ggNMOS ESD protection device utilizing the DET has been investigated. Since the area-component occupies more than 90% of C_j in the ggNMOS, the DET realizes almost 1/3 reduction of C_j. Performing TLP testing, it has been confirmed that the DET features about the same or higher It2 as compared with the conventional. To obtain an It2 of 1-1.33A corresponding to an HBM robustness of 2kV, only a low C_j of less than 150fF is needed. The proposed ESD protection device is very promising for realization of high-performance and highly reliable RF CMOS IC's.

Acknowledgments

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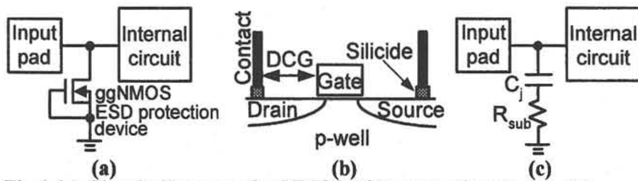

Fig.1 (a) Circuit diagram of ggNMOS ESD protection device, (b) schematic illustration of its cross-section, and (c) its equivalent circuit.

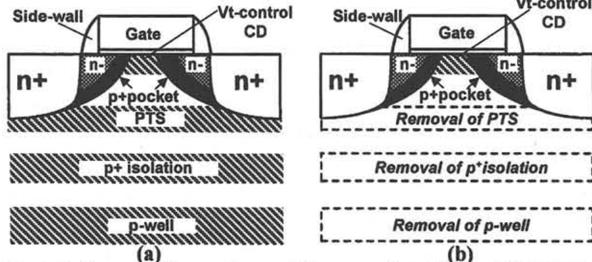

Fig.2 Schematic illustrations of (a)conventional Tr and (b)DET.

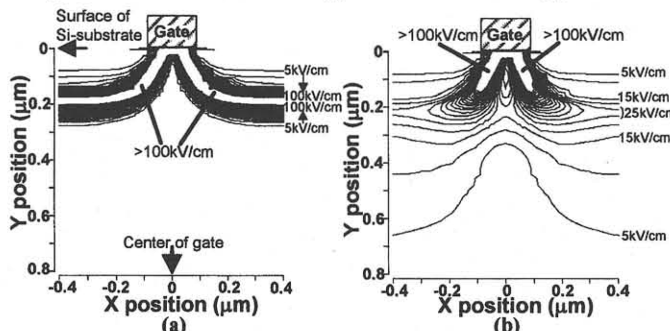

Fig.4 Device simulation results of electric field strength in NMOS-Trs in non-bias condition. (a) 2D profile in the case of conventional Tr, (b) 2D profile in the case of DET.

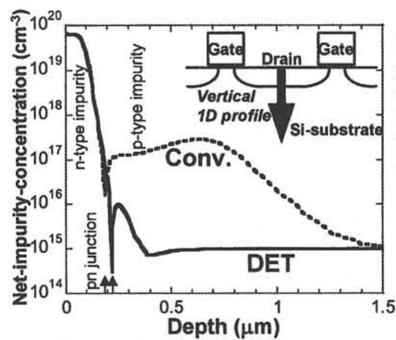

Fig.3 Simulated 1D vertical profiles of net-impurity-concentration at the center of S/D region of DET as compared with conventional(conv.) Tr.

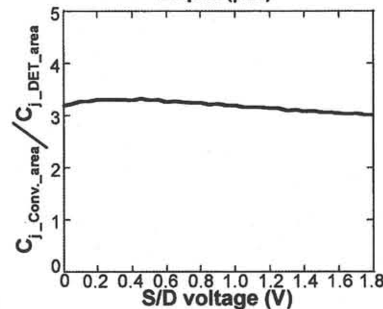

Fig.5 Voltage dependence on reduction ratio in area-component of C_j of DET as compared with conventional Tr.
Reduction ratio is defined as $C_{j_Conv._area} / C_{j_DET_area}$. Here, $C_{j_Conv._area}$ is C_j area-component of conventional Tr and $C_{j_DET_area}$ is C_j area-component of DET.

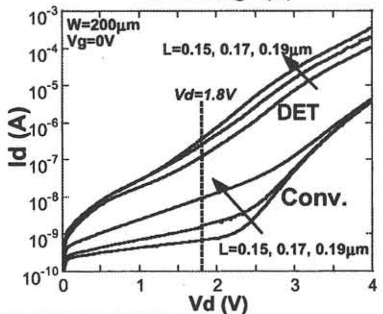

Fig.6 L dependence on off-leakage current characteristics. Although off-leakage current of DET is increased by about two orders, L dependence on its off-leakage current characteristics is very stable. This is because p⁺pocket-layer strictly limits lateral punch-through current in regions shallower than junction position.

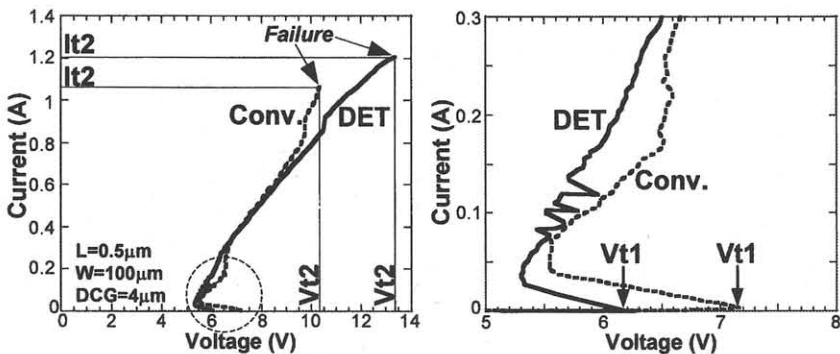

Fig.7 (a) TLP characteristics of DET as compared with conventional Tr, and (b) magnified figure of dashed-circle region in Fig.7(a). It2 of DET is about the same or higher than that of conventional Tr (Fig.7(a)). Vt1 of DET is reduced by 1V as compared with conventional Tr (Fig.7(b)).

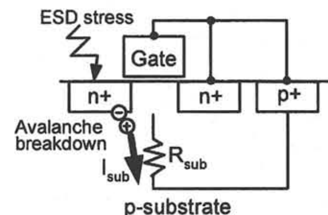

Fig.8 Schematic illustration of parasitic bipolar action of ggNMOS during ESD stress. During ESD stress, avalanche breakdown occurs in drain, and substrate current (I_{sub}) flows to substrate. Here, in substrate resistance of R_{sub}, a voltage-drop of $I_{sub} \cdot R_{sub}$ is generated. As this voltage-drop reaches 0.7V, a parasitic bipolar transistor via substrate turns on.

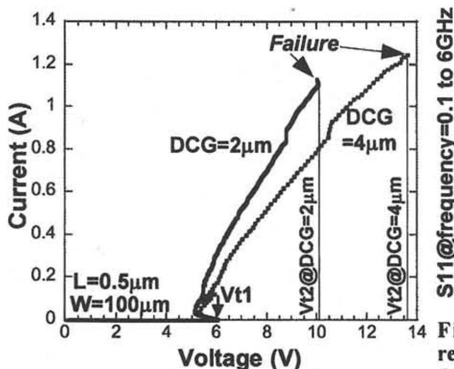

Fig.9 Contact to gate spacing(DCG) dependence on TLP characteristics of DET.

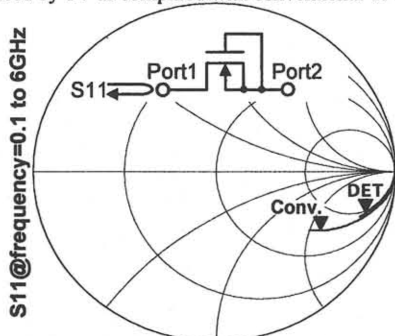

Fig.10 Smith-chart plot of input reflection s-parameters(S11) of ggNMOS devices of DCG=2μm and W=100μm in cases of DET and conventional Tr. Markers are positioned at 5GHz.

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