

**A-4-1 (Invited)****MOSFET Channel Engineering using Strained Si, SiGe, and Ge Channels**

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**1. Introduction**

Epitaxial relaxed SiGe buffer layers [1] create a larger lattice constant on a Si substrate, allowing subsequent SiGe layers to be strained in tension or compression. Early work in application of strain via relaxed SiGe concentrated on investigating elevated carrier mobility in pure tensile Si layers deposited on relaxed Si<sub>1-x</sub>Ge<sub>x</sub>. [2][3]. Relatively short channel MOSFETs containing strained Si have shown that higher mobility and drain current measured in long channel devices are retained at shorter channel lengths. [4][5] A quantitative method to correlate the effect of mobility enhancement in long and short channels shows that approximately 50% of the long channel drain current enhancement is obtained in shorter channels. [6] Thus, large MOSFET devices can be used to rapidly probe heterostructures for channel enhancement, as well as limits to processing. [7][8] In this summary, we report on probing advanced SiGe heterostructures to understand the potential of strained Si/SiGe heterostructures in MOSFETs. We also show that commercially produced strained Si materials can be processed in a 0.13 $\mu$ m node CMOS process, demonstrating that these materials can withstand CMOS process conditions and produce NMOS transistors with 40% current drive enhancement as compared to control Si NMOS transistors.

**2. Single Strained Si Channels on Relaxed Si<sub>1-x</sub>Ge<sub>x</sub>**

Tensile strain in Si increases the mobility of electrons nearly 80% over that in conventional MOS channels. [4][7] Holes also have increased mobility in strained Si; however, greater strain levels in the strained Si are required to achieve the same hole mobility enhancement as achieved for electrons. Also, hole mobility enhancement does not saturate as readily as the electron case. Fig. 1 shows the carrier mobility enhancement factors for electrons and holes as a function of Ge concentration in the relaxed Si<sub>1-x</sub>Ge<sub>x</sub>. The data are extracted from one-mask-step large gate length MOSFETs that have vertical electric fields in the channel comparable to MOSFETs with shorter gate lengths. The data for x<0.5 are from references [7][8].

We report that significant mobility enhancement (enhancement factor 2.5) in PMOS devices can continue to increase in single strained Si layers with x>0.5. Planar strained Si layers (partially relaxed through the introduction of dislocations) have been achieved on all buffer layer

compositions, including pure Ge by very low temperature chemical vapor deposition (T<=400C).

**3. Dual Channel Heterostructures on Relaxed Si<sub>1-x</sub>Ge<sub>x</sub>**

Although hole mobility enhancements of 2.5 are even larger than the maximum electron mobility enhancement, we have shown that incorporating a compressively strained Si<sub>1-x</sub>Ge<sub>x</sub> layer below the tensile-strained surface Si layer increases the hole mobility to an even greater extent, without impacting electron enhancements. [9] Such dual channel heterostructures have shown hole mobility enhancement factors in PMOSFETs as high as 8 at vertical fields of 0.65 MV/cm (with little sign of degradation as field is increased) for a structure of pure Si and pure Ge layers deposited on x=0.7. [10] Fig. 1 summarizes the best carrier mobility enhancements in large research MOSFETs achieved to date for different heterostructures on relaxed Si<sub>1-x</sub>Ge<sub>x</sub> on Si.

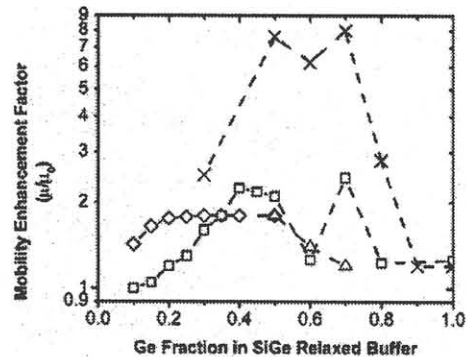


Fig. 1 Summary of mobility enhancements extracted from one-mask-level, large MOSFETs with a vertical effective field of approximately 0.6 MV/cm: single channel NMOS (diamonds), single channel PMOS (squares), dual channel NMOS (triangles), dual channel PMOS (crosses).

**4. Digital Alloy Channels**

Combining the single channel and dual channel data, we speculate that the heterostructures in many of the PMOS devices have a thickness less than the vertical extent of the hole wavefunction and therefore the properties of the hole is determined by a combination of the hole wavefunction in the gate dielectric, the strained Si, the compressed Si<sub>1-x</sub>Ge<sub>x</sub> (if present), and the relaxed Si<sub>1-x</sub>Ge<sub>x</sub> alloy. Layer thickness and vertical electric field are variables in determining the character of the hole wavefunction in the channel. To further elucidate this observation, we have built a digital

alloy channel (greater than 100Å in total channel thickness) composed of extremely thin layers of tensile Si and Si<sub>0.3</sub>Ge<sub>0.7</sub> on a relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub> substrate (see Fig.2).

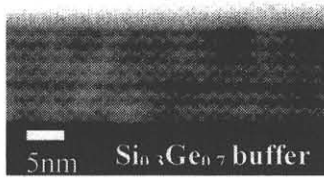


Fig. 2 Cross-section TEM of digital alloy channel. Bright layers are ε-Si, dark layers are Si<sub>0.3</sub>Ge<sub>0.7</sub>

In this way, we have ‘mixed’ the top surface Si in our single channel Si/ Si<sub>0.3</sub>Ge<sub>0.7</sub> structure with the buried relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub>. The PMOSFETs fabricated from this material show that the mobility enhancement factor (2.1) is independent of vertical field, as expected since the wavefunction is averaging over all of the digital alloy layers at all electric field values. We also note that compositionally, the digital alloy is equivalent to a tensile x=0.3 alloy on relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub>, which has been shown to have a degraded mobility.[8]

### 5. Single Channel Strained Si in Commercial CMOS Process

Although the previous sections show that heterostructure MOS has great potential due to enhanced carrier transport in the channel, only the channel is probed by the research structures described in the previous sections. Many materials and process issues are encountered on the path to creating commercial strained Si material and fully processed MOSFETs. Here, we report high quality, commercially available strained Si on x=0.2 has been processed in a 0.13 μm process node, resulting in NMOS drive current enhancements of over 40%. Fig. 3 is a TEM cross-section of 90nm physical gate length 0.13 μm node strained Si NMOSFET. The strained Si channel is preserved throughout the CMOS process, and the gate is comprised of a nitrated 16Å-thick oxide. Fig. 4 shows long channel (W/L=10μm/10μm) device characteristics, showing a 43% enhancement in NMOSFET current drive. The Si control and the strained Si device have the same V<sub>t</sub>. g<sub>m</sub> increases by 61%. Thus, high quality strained Si material can be processed in a full, slightly modified CMOS process.

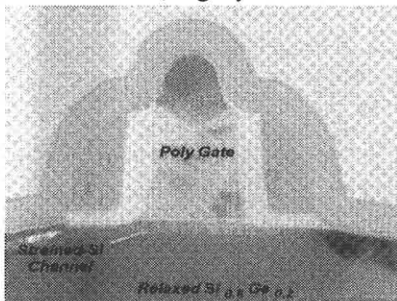


Fig. 3 Cross-section TEM of a 0.13μm-node, 90nm physical gate length strained Si NMOSFET.

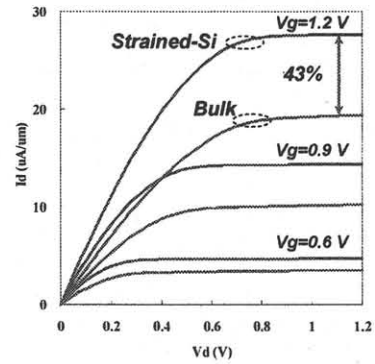


Fig. 9 Transistor characteristics from W/L 10μm/10μm fully CMOS processed 0.13μm-node strained Si NMOSFET.

### 6. Conclusions

Short flow, one-mask-step large MOSFETs have been used to explore the potential of heterostructure CMOS channels. Electron mobility enhancements as high as 1.8 and hole enhancements of over 8 have been achieved. Digital alloy channels have enhanced our understanding of hole wavefunctions in these heterostructures. Strained Si channels have been processed in real CMOS manufacturing environments, delivering the expected enhancements in processed MOSFETs.

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### References

- [1] E. A. Fitzgerald, Y. H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. J. Mii, B. E. Weir, Applied Physics Letters, vol. 59, no. 7, pp. 811-813 (1991).
- [2] Y. J. Mii, Y. H. Xie, E. A. Fitzgerald, D. Monroe, F. A. Thiel, B. E. Weir, L. C. Feldman, Applied Physics Letters, vol. 59, no. 13, pp. 1611-1613, (1991).
- [3] F. Schaffler, D. Tobben, H.J. Herzog, G. Abstreiter, and B. Hollander, Semicond. Sci. Technol., vol. 7, p. 260, 1992.
- [4] J. Welsler, J. L. Hoyt, J. F. Gibbons, IEEE Trans. Electron Dev., vol. 40, no. 11, p. 2101, 1993.
- [5] K. Rim, J.L. Hoyt, and J.F. Gibbons, IEEE Trans. Electron Devices 47, 1406 (2000).
- [6] A. Lochtefeld and D.A. Antoniadis, IEEE Electron Dev. Lett., vol. 22, no. 12, pp. 591-593 (2001).
- [7] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, J. Vac. Sci. Technol. B, vol. 19, no. 6, pp. 2268-2279 (2001).
- [8] C.W. Leitz, M.T. Currie, M.L. Lee, Z.-Y. Cheng, D.A. Antoniadis, and E.A. Fitzgerald, J. Appl. Physics (in print, scheduled publication September 15, 2002).
- [9] C. W. Leitz, M. T. Currie, M. L. Lee, Z.-Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald, Appl. Phys. Lett., vol. 79, no. 25, pp. 4246-4248 (2001).
- [10] M. L. Lee, C. W. Leitz, Z.-Y. Cheng, A. Pitera, T. A. Langdo, M. T. Currie, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, Appl. Phys. Lett., vol. 79, no. 20, pp. 3344-3346 (2001).