

A-4-3

Realization of dislocation-free relaxed SiGe-on-Insulator substrates by mesa isolation

Tsutomu Tezuka, Naoharu Sugiyama and Shinich Takagi

MIRAI-Project, Association of Super-Advanced Electronics Technology (ASET)
Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan
Phone: 044-549-8217, Fax: 044-549-8216, e-mail: tez@mirai.aist.go.jp

1. Introduction

Strained Si-on-Insulator (SSOI) MOSFETs on (001) relaxed SiGe-on-Insulator (SGOI) substrates are promising devices for high-performance CMOS circuits, because of high carrier mobilities and low parasitic capacitances [1]. In order to scale down SSOI-MOSFETs, SGOI layers are required to be thin enough to reduce the short-channel effect for a fully-depleted (FD) mode operation. Recently, we have proposed an SGOI fabrication technique based on Ge-condensation by high-temperature oxidation of SiGe/SOI layers [2]. While this is an attractive technique for thin (<100 nm) SGOI layers, the strain relaxation of such thin layers have been limited up to 50%. In addition, the layer had slightly undulated surfaces and considerable amount of dislocations. In this paper, we propose a new Ge-condensation technique combined with mesa isolation, and demonstrate completely relaxed thin SGOI substrates without dislocations and surface undulations for FD-SSOI CMOS applications.

2. SGOI fabrication

In order to enhance the relaxation, mesa isolation before the oxidation may be effective, because the free edge around the mesa helps the lateral expansion. The proposed SGOI fabrication procedure with the mesa isolation is shown in Fig.1 (a)-(c). First, a pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ layer of the initial thicknesses, T_i , is epitaxially grown on an SOI wafer (a). Next, mesas for the active region of the MOSFETs are defined by chemical dry etching, (b). Finally, these mesas are dry-oxidized at temperatures higher than 1000°C, (c). When the layers are thinned down to the final thickness, T_f , the Ge fraction in the SGOI layers is increased up to $x=x_0(T_i/T_f)$. This is because Ge atoms are pushed into the SGOI layer from the oxidized layer, whereas the oxide layers suppress the Ge diffusion out of the SGOI mesas [2]. The mesas are relaxed during the oxidation via the mesa edges.

3. Structural analysis and relaxation mechanism

Plan view and cross section TEM images in Fig. 2 for the mesa of the radius, R , of 2.3 μm and T_f of 95 nm after oxidation exhibit no dislocation in the SGOI layers. The EDX measurements revealed that the Ge fraction was increased up to $x=0.15$ from $x_0=0.1$. The Raman spectrum of the mesa in Fig. 3 indicates strain relaxation at the center of the mesa, in which the peaks for Si-Si and Si-Ge vibration modes deviate from those for the strained SGOI mesa. The relaxation ratio, γ , was evaluated from the pairs of the Raman

peak values [3], and plotted in Fig. 4. It was found that the strain relaxation was enhanced for smaller and thicker mesas, and for higher oxidation temperature. Considering the application to MOSFETs of 70-nm generation and beyond, relaxed SGOI mesas smaller than 1 μm^2 are desirable. For such small mesas, complete relaxation has been confirmed up to $x=0.35$ using this technique (Fig. 5). The radial strain-distribution in the mesa (Fig. 6) indicates that the relaxation takes place from the peripheral region and proceeds into the central region via a slip at the interface between the SGOI and buried oxide (BOX) layers. It was also found that the relaxed smaller mesas exhibited smooth surface without undulations (Fig. 7). The roughness *rms* value was improved up to 0.17 nm for the SGOI mesa of $R=1.9 \mu\text{m}$. This is the result of the efficient strain release during the Ge-condensation process.

The relaxation mechanism was modeled by a 2D-stress balance model, which resulted in the relation, $\varepsilon_c \propto R \tau_{slip}/T$. Here, ε_c , τ_{slip} and T represent the strain at the center of the mesa, the critical share stress for the onset of the slip at the SGOI/BOX interface and the mesa thickness, respectively. This model was verified by the linear dependences of ε_c on R in Fig. 8, as well as larger γ for the thicker mesas in Fig. 4. According to this model, the temperature dependences of γ in Fig. 4 can be explained by a smaller τ_{slip} value at a higher temperature. It was found that the value of τ_{slip} for 1200°C was only 1/10 of that for 1050°C, which were extracted from the slopes of the strain dependences in Fig. 8. This may be due to enhanced slip at the interface by a plastic deformation of SiO_2 at the higher temperature.

4. Conclusions

Relaxed SGOI mesas without dislocation and surface undulation were successfully fabricated using a mesa etching followed by a high-temperature oxidation of SiGe/SOI layers. It is concluded that ideal SGOI layers for high performance SSOI-CMOS can be fabricated by this technique with minimum change of conventional SOI-CMOS processes.

Acknowledgments

The authors are grateful to T. Kawakubo, H. Satake, K. Usuda and M. Hiramatsu for fruitful discussion and technical support. This work was partly supported by NEDO.

References

- [1] T. Mizuno et al., IEDM Tech. Dig., 934 (1999).
- [2] T. Tezuka et al., Appl. Phys. Lett. **79**, 1798 (2001).
- [3] J. C. Tsang et al., J. Appl. Phys. **75**, 8098 (1994).

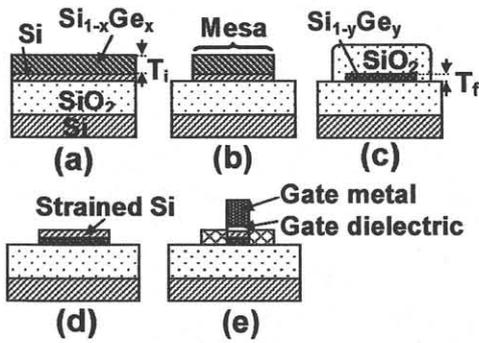


Fig. 1 Fabrication procedure of a SGOI mesa structure, (a)-(c), and a strained SOI-MOSFET on it, (d), (e). Typical thickness of the starting SOI layer is 30 nm.

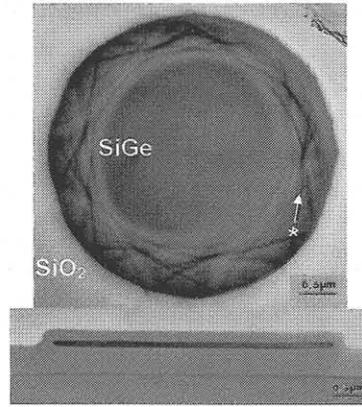


Fig. 2 Plan view and cross section TEM images of the SGOI mesa after oxidation at 1200°C. The initial Ge fraction of 0.1 was increased up to 0.15 associated with a decrease in thickness from 137 nm to 95 nm. The periodic interference pattern (*) is due to a slight thickness variation around the peripheral.

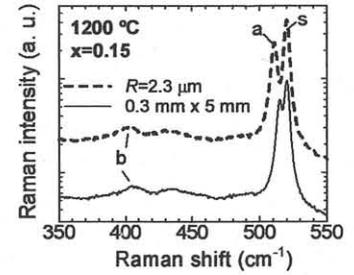


Fig. 3 Raman spectrum for the SGOI mesa shown in Fig. 2 ($R=2.3 \mu\text{m}$, broken line) and the large mesa as a reference ($0.3 \text{ mm} \times 5 \text{ mm}$, solid line). Raman peaks indicated by *a*, *b* and *s* are assigned to be a Si-Si mode in SiGe, a Si-Ge mode in SiGe and a Si-Si mode in Si. The laser beam was focused into diameter of $1 \mu\text{m}$ on the centers of the mesas.

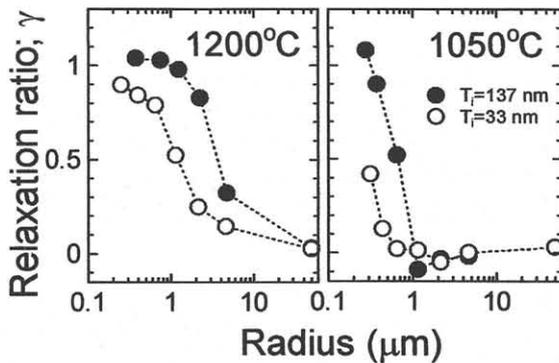


Fig. 4 Relaxation ratio, γ , for SGOI mesas ($x=0.15-0.22$) as a function of the mesa radius, which is evaluated from pairs of the Raman peak positions corresponding to a Si-Si and a Si-Ge modes in the SGOI layer. The solid and open circles indicate the obtained relaxation ratio for the mesas with the initial SiGe thicknesses $T_i=137 \text{ nm}$ and 33 nm , respectively. Here, the relaxation ratio was defined as $1-\epsilon_c/(\epsilon_c\epsilon_0)$, where ϵ_c is the strain at the center of the SGOI mesas, and ϵ_0 is the strain in a pseudomorphic Ge layer grown on a Si substrate.

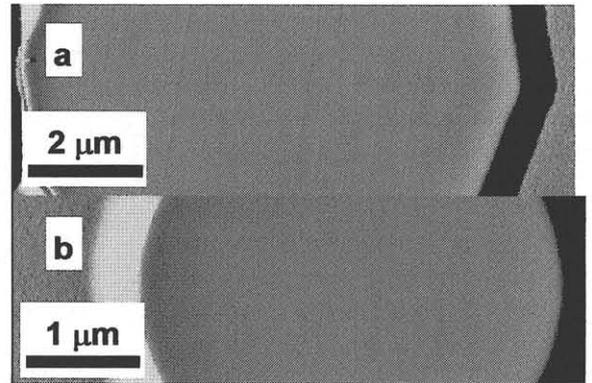


Fig. 7 Tapping mode AFM images (differential images) for the SGOI mesas of $R=4.4 \mu\text{m}$, (a), and $R=1.9 \mu\text{m}$, (b), after removal of the surface oxide layers. The Ge fraction is $x=0.26$ for both mesas.

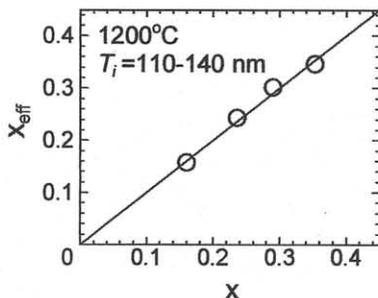


Fig. 5 Effective Ge fraction, $x_{\text{eff}}=\gamma x$, for smaller SGOI mesas of $0.5 \mu\text{m} < R < 1.3 \mu\text{m}$ as a function of x . The solid line indicates a condition of complete relaxation of SiGe, i.e., $\gamma=1$.

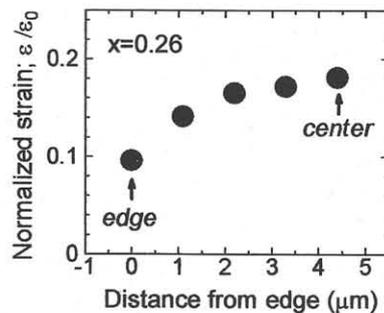


Fig. 6 Strain distribution along the radial direction for the SGOI mesa of $R=4.4 \mu\text{m}$ evaluated from Raman measurements. The strain, ϵ , is normalized by that for pseudomorphic Ge layer grown on a Si substrate, ϵ_0 .

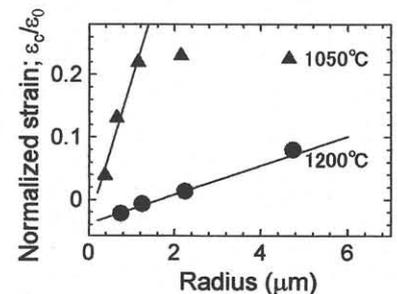


Fig. 8 Normalized strain for SGOI mesas of $T_i=137 \text{ nm}$ at the centers. The Ge fraction is $x=0.15$ after oxidation at 1200°C , and $x=0.22$ at 1050°C . Evaluated τ_{slip} values from the slope of the linear fits are $8.4 \times 10^7 \text{ N/m}^2$ for 1200°C and $8.1 \times 10^8 \text{ N/m}^2$ for 1050°C .