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Low-Temperature Electrical Characteristics of Strained-Si MOSFETs

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The strained-Si MOSFET is attracting much attention these days because of its high electron and hole mobilities. Many research groups have enhanced the performance of this device [1, 2]. We previously reported large increases in mobility of electrons and holes (120% and 42%, respectively) compared to a conventional Si-MOSFET in a strained-Si MOSFET with a chemo-mechanical polished SiGe substrate [3]. There have been many theoretical investigations on the mechanism of the increase in mobility [4, 5], although a discrepancy between experimental and theoretical values still exists. It is necessary to investigate mobility-limiting mechanisms of the strained-Si MOSFET. Useful information can be gained from mobility measurements at low-temperature. But there are few reports on the low-temperature mobility [6]. Accordingly, in this study, we investigated temperature dependence of both electron and hole mobilities in a strained-Si MOSFET.

Details of the device fabrication are described elsewhere [3]. Channel-doping density was around $4\times10^{17}/cm^3$. The gate-oxide thickness was 4 nm, and n^+- and p^+- poly-Si gate electrodes were used. Electrical characteristics of the devices were measured by using a low-temperature wafer prober in a temperature range of 83-300 K.

The I_d-V_{gs} characteristics of the strained-Si devices with L_g of 0.8 μm are shown in Fig. 1. With decreasing temperature, threshold voltage $|V_{th}|$ decreases, and on-state I_d and sub-threshold slope (S) increase. The $|V_{th}|$ values of all the devices at 83 K are approximately 0.2 V higher than those at 300 K. This result is consistent with that from device modeling at low temperatures [7]. High-frequency (1 MHz) C-V characteristics of the strained-Si nMOS capacitor are shown in Fig. 2. Accumulation-state capacitance (V<-2 V) increases a little with decreasing temperature. This increase suggests that gate-oxide capacitance slightly (<5%) increases with decreasing temperature. Since minimum capacitances among all the devices under a depletion-inversion state (V>-0.5 V) are identical and do not depend on temperature, the space charges of all the devices seem to be the same and independent of temperature. Figure 3 shows temperature dependence of S for devices with L_g of 0.8 μm. If space charge and interface-trap charge densities are constant, S should be proportional to temperature. The result indicates that interface-charge densities of all the devices are almost the same because their space-charge densities are the same. The interface state between the gate oxide and the strained-Si channel therefore seems to be the same as that for conventional Si devices.

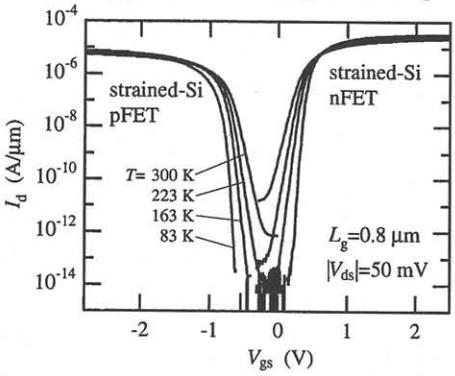

Fig. 1 I_d-V_{gs} characteristics of strained-Si MOSFETss with L_g=0.8 μm.

Figures 4-7 show electron and hole mobilities (μ_{eff}) as a function of effective electric field (E_{eff}). At 300 K, μ_{eff} in the Si control devices is identical to the universal values [8] under high E_{eff} (>0.8 MV/cm). This indicates that mobilities are mainly limited by phonon and surface-roughness scattering. With decreasing temperature, μ_{eff} increases because the contribution of phonon scattering decreases. But in the nFETs, unlike the results in the literature [8], the contribution of surface-roughness scattering (E_{eff}^{-2}) is still weak below 100 K. This may be because the contribution of Coulomb scattering is strong because of high channel-doping density. Mobilities of the strained-Si devices are higher than those of the conventional ones throughout the measured temperature range.

Mobility-enhancement ratio of the strained-Si devices over corresponding conventional-Si devices is plotted in Fig. 8. Surprisingly, the enhancement ratio does not significantly decrease with decreasing temperature; on the contrary, the

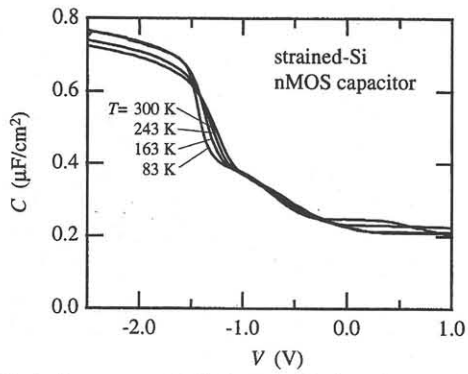

Fig. 2 High-frequency C-V characteristics of a strained-Si nMOS capacitor.

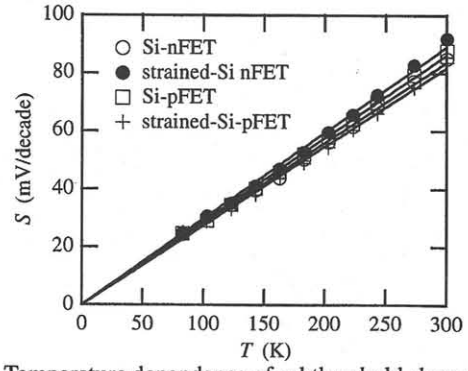

Fig. 3 Temperature dependence of subthreshold slope (S) of the L_g=0.8 μm devices.

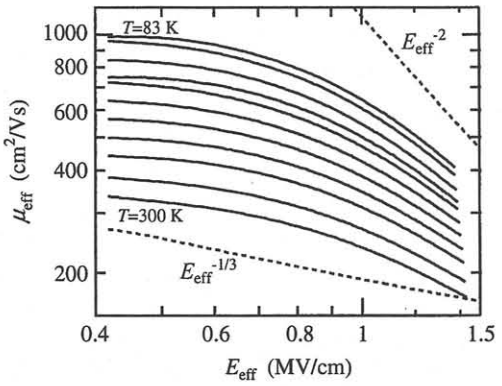

Fig. 4 Electron mobilities (μ_{eff}) of Si control devices as a function of effective electric field (E_{eff}). Measurements were done at 83, 103, 123, 143, 163, 183, 203, 223, 243, 273, and 300 K.

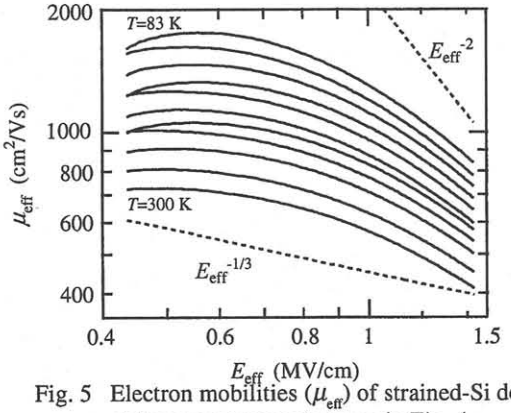

Fig. 5 Electron mobilities (μ_{eff}) of strained-Si devices at the same temperatures as in Fig. 4.

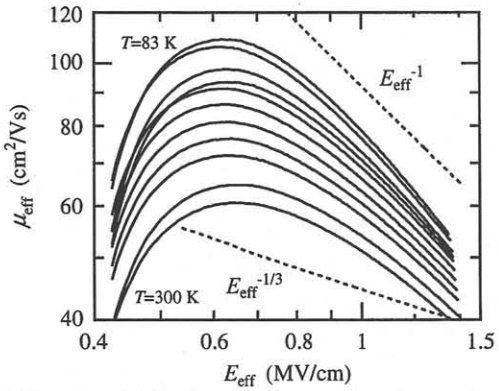

Fig. 6 Hole mobilities (μ_{eff}) of Si control devices at the same temperatures as in Fig. 4.

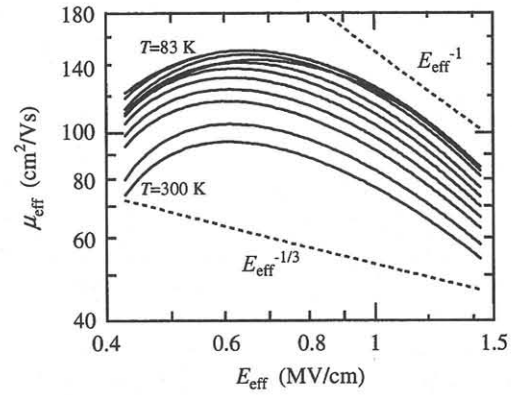

Fig. 7 Hole mobilities (μ_{eff}) of strained-Si devices at the same temperatures as in Fig. 4.

ratio for holes increases slightly ($E_{eff} \geq 1$ MV/cm). As explained in the literature [4, 9], if the electron-mobility enhancement is due to a decrease of the inter-valley phonon scattering, the electron-mobility enhancement should be less than 10% below 100 K. Moreover, under a high electric field ($E_{eff} \geq 1$ MV/cm), the enhancement should be small [9], even at room temperature, because the two dimensionality of the inversion layer is enhanced with increasing E_{eff}, and the reduction of the inter-valley scattering occurs even in the conventional Si devices. Thus, the present experimental results cannot be explained only by the mechanism reported so far. Further investigations such as mobility measurements with different channel-dose amounts, as well as theoretical investigations of mobility-limiting mechanisms of strained-Si devices, are necessary.

In summary, we measured low-temperature electrical characteristics of strained-Si MOSFETs in order to understand the mobility-limiting mechanism in this device. We found that, unlike previous theoretical investigations, both the electron and hole mobilities do not significantly decrease with decreasing temperature. These results cannot be explained by the mechanisms reported so far; namely, electron-mobility enhancement is not only caused by the reduction of phonon scattering by the valley splitting.

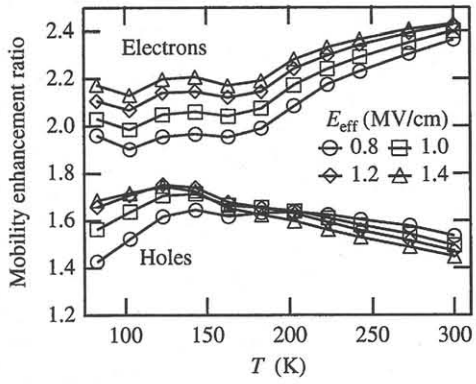

Fig. 8 Temperature dependence of mobility-enhancement ratio of strained-Si devices over corresponding conventional Si devices.

Acknowledgments

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