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Enhanced Tunneling Current Effect for Nonvolatile Memory Applications

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1. Introduction

Flash memory technology arrived at a point where the downscaling of the tunnel dielectric reached the limits imposed by reliability specifications. In order to further improve its performances in terms of programming speed and/or decrease of the operating voltages, new concepts are required. The SIA roadmap [1] points to tunnel barrier/dielectric engineering as one of the possible routes to overcome these limitations. In this work, enhancement of the tunneling current is demonstrated by using a "dielectric constant effect" present in two-layer tunnel dielectric stacks. We also confirm these predictions by means of experimentally observed data.

2. Theoretical Results

The independent electron approximation [2] has been used to calculate the tunneling current through double-layer stacks. Ideal dielectric materials have been considered, with a piecewise linear shape of the barrier profile. The tunneling probability has been calculated using a transfer matrix formalism and an approach based on Airy functions [3].

In most cases, deposition of high-k dielectrics requires that an interfacial SiO_2 layer exists between the silicon substrate and the high-k dielectric. Consequently, the analysis of the tunnel currents through asymmetric layers consisting of one layer of SiO_2 and one layer of a high-k dielectric on top of it is of practical importance. There are several candidate high-k materials to replace the conventional CMOS gate dielectric. Their parameters, relevant for the electrical performance, are only roughly known [4] and in fact, we have learnt that they depend on many factors, including e.g. processing history. Thus, a quantitative evaluation of their impact on tunneling performances is necessary.

Two-layer stacks of fixed physical thickness have been considered. We evaluated the influence of the high-k material parameters on the tunneling current. The thickness of the SiO_2 layer is 3 nm, and a barrier height of 3.1 eV has been assumed. The high-k dielectric had a thickness of 10 nm, whereas the dielectric constant and the barrier height of the high-k material have been sequentially considered as variable parameters within the range of values common to the most promising candidate high-k materials for SiO_2 replacement [4].

Influence of the high-k barrier height

Plots of the tunnel current density (J_g) against stack voltage drop (V_d) in Fig. 1,a show a shoulder beyond which the slope of the current density changes significantly. The tunnel current density decreases very sharply with the dielectric voltage for voltages below this transition region, since both dielectric layers effectively exhibit a barrier for the tunneling electrons. Moreover, for high V_d, the tunneling current is nearly identical irrespective of the high-k barrier value, which is due to the fact that the potential profile of the SiO_2 layer does not depend on the value of the high-k barrier height. The IV shoulder is assigned to the transition from tunneling through a two-layer barrier to tunneling through a single-layer barrier. When increasing the barrier height of the high-k layer, the IV shoulder also moves to higher voltage values.

Influence of the high-k dielectric constant

By contrast, when the dielectric constant of the second layer is considered as a parameter, the effect on the tunneling current is not only reflected in the location of the transition region, but also in the slope and magnitude of the current: a steeper slope is obtained at low voltages for higher dielectric constants. Moreover, the current increases with the dielectric constant over the entire voltage range (Fig. 1,b). This is due to the fact that a higher dielectric constant of the high-k layer forces a larger fraction of the stack voltage to drop across the SiO_2 layer determining a faster decrease of the barrier with the applied bias.

Band diagrams: The VARIOT effect

This behavior can also be understood by examining the band diagrams of the barrier at different biases. A transition voltage (V_{tr}) can be associated with the bending of the IV curves, which can be derived from basic electrostatics when imposing the condition that the voltage drop across the SiO_2 layer equals the barrier height of the high-k layer,

$$V_{tr} = \left(1 + \frac{t_{hk}}{t_{ox}} \cdot \frac{k_{ox}}{k_{hk}}\right) \cdot \Phi_{B,hk} \qquad (1)$$

and essentially represents the stack voltage drop beyond which the tunneling current is controlled by the first layer of the stack only (Fig. 2).

At low biases, the tunneling barrier is formed by both the SiO_2 and the high-k dielectric. A high dielectric constant of the high-k material allows for thick physical thickness, which reduces the tunneling current. When applying a voltage to the stack, this voltage is distributed over the two layers inversely proportional to their dielectric constant, i.e. the higher the high-k dielectric constant, the higher the oxide voltage drop. Since the high-k material usually has a lower barrier height, the barrier shown by the double-layer stack is more transparent than the barrier of an SiO_2 layer of identical electrical thickness (EOT) at voltages around V_{tr}. Ultimately, when the applied bias is very large, the tunneling current through the stack is identical to the tunneling current through the thinner EOT layer [5]. In this view, the double-layer stack can be regarded as a VARIable Oxide Thickness (VARIOT) layer [6].

Nonvolatile memory opportunities

The VARIOT concept opens opportunities for nonvolatile memory applications: a higher programming speed, i.e. as high as (or higher than) the speed that would be obtained by

tunneling through a thin EOT layer at identical large biases (or biases around V_{tr}) can be achieved. Alternatively, lower voltage programming at identical speed is possible. The thicker physical thickness of the stack offers better retention performances as compared to the EOT layer. Eq. (1) can also be used to explain the shape of the tunneling current when the layer thicknesses change. In order to obtain higher programming speed with such structures, the tunneling current must be as high as possible at large biases, which requires that the thickness of the first layer should be small, yet its presence is crucial to modulate the shape of the barrier. To reduce the programming voltage, a large fraction of the applied voltage should drop over the first dielectric layer, for which a small k_{ox}/k_{hk} ratio is needed. The barrier height is mainly important in controlling the position of the transition point. If the barrier height of the second layer were too low, this would lead to too large currents at low biases, hence adversely affecting the retention.

3. Experimental Correlations

Different area MOS capacitors have been fabricated on either lowly or highly doped n-type (100) Si substrate. The gate stack consists of a SiO_2 layer and a ZrO_2 layer deposited by ALCVD. The top electrode is PVD TiN. The wafers received no post-deposition anneal. Capacitors have been subjected to standard characterization techniques. The HFCV technique has been used to extract the electrical thickness (EOT) [7] from lowly doped substrate capacitors. Regression slope of the EOT versus t_{hk} for capacitors with identical oxide thickness allowed for estimation of k_{hk}=23.6. The simulated IV curves (substrate injection) are shown in Fig. 4 against measured data, for stacks having 2.95 nm optical thickness SiO_2 and different ZrO_2 thicknesses, i.e. 8, 12, 16 and 20 nm. The same set of high-k parameters (k_{hk}=23.6, $e\Phi_{B,hk}$=1.5 eV) has been used for simulating all stacks. A good agreement between simulation and measurement is observed for a large voltage bias range, suggesting that in this region the dominant conduction mechanism could be tunneling. There are however some differences, both in the low as well as very high gate bias regions. In the low gate bias range, both dielectric layers effectively show a barrier to the tunneling electron. Assuming that the high-k material has traps, these would allow for more effective conduction paths, the measured current thus exceeding the tunneling component. In the high bias range, the tunneling current predicted by simulations is systematically larger than the measured current. This could be due to the fact that the negative charge trapped in the high-k dielectric reduces the SiO_2 field, building up an additional tunneling barrier (This assumption has been verified by double sweep IV and CV measurements.).

Calculation of the transition voltage from two-layer to single-layer tunneling shows that an important part of the region of good agreement corresponds to a single-layer tunneling current (Fig. 3), i.e. conduction is limited by the SiO_2 layer. Furthermore, J_g plots as a function of the SiO_2 voltage drop showed that in the single layer conduction region the current curves fall on top of each other (plot not shown), suggesting that the conduction is controlled by the SiO_2 layer.

4. Conclusion

We analyzed the influence of the main high-k material parameters on the tunneling current of double-layer stacks. Requirements to enhance tunneling for achieving higher programming speed or lower voltage for nonvolatile memory operation have been discussed. The most promising two-layer combination with SiO_2 as one of the layers would require a material with moderate barrier height and a significantly higher dielectric constant as compared to SiO_2. Experimental results suggest that the conduction is mainly controlled by the SiO_2 layer over the voltage range of interest for programming.

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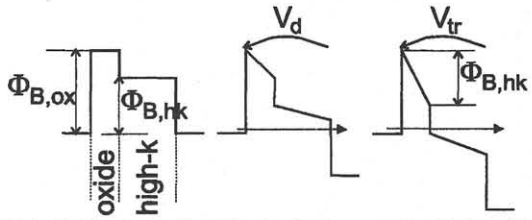

Fig. 2: Potential barrier profile of the double-layer stack at flatband (left), at a particular voltage drop across stack V_d, corresponding to two-layer tunneling (middle) and at the transition voltage V_{tr} (right). For simplicity, identical electrodes have been assumed in these drawings.

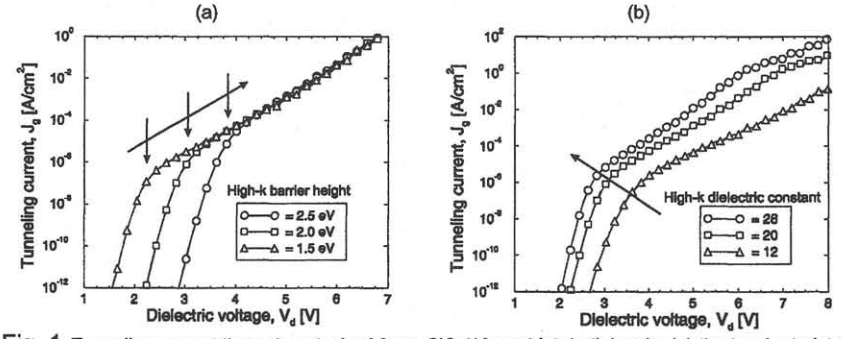

Fig. 1: Tunneling current through a stack of 3 nm SiO_2/10 nm high-k dielectric: (a) the barrier height of the high-k is the variable parameter and k_{hk}=20 (fixed); (b) the dielectric constant of the high-k is the variable parameter and $\Phi_{B,hk}$=2.0 V (fixed). Usual parameters have been assumed for SiO_2. The solid line arrow indicates the variation of the transition voltage V_{tr} with increasing variable parameter.

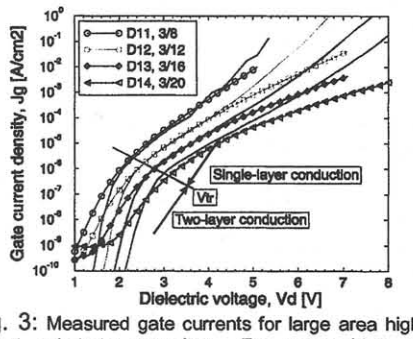

Fig. 3: Measured gate currents for large area highly doped substrate capacitors. For comparison, the calculated tunneling current is also shown. The transition voltage has been calculated using eq. (1).