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Flash Memory Reliability: an improvement against Erratic Erase phenomena using the Constant Charge Erasing Scheme.

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I. Introduction

Flash memory reliability has grown in parallel with the understanding of the physical mechanisms responsible for anomalous phenomena occurring during program and erase operations. One of these mechanisms, the erratic erase, consists in statistical fluctuations of the Fowler-Nordheim (FN) cell parameters that produces different erased threshold voltages after two consecutive program/erase cycles [1]. Since it first appearance [2], it has always been stated that, due to its statistical nature, this problem must be taken into account at the design level (e.g. using softprogramming for threshold voltage recovery). Up to now, no particular studies have been made in order to reduce its statistical occurrence during cycling using suitable erasing schemes. The experimental results, shown in this work, demonstrate that the erratic erase phenomenon may be drastically reduced switching from a standard box erasing scheme to a constant charge erasing scheme. This result improves the flash memory reliability reducing the erratic bit failure and lowers, at the same time, the workload supported by any threshold recovery method.

II. Measurement setup

Nine different virgin sectors (A-I) of 512kbits featuring 10.2nm tunnel oxide have been cycled for 10,000 cycles.

Programming was performed via channel hot electrons by applying one single rectangular gate-to-bulk and drain-to-bulk pulse.

Erasing was performed using two different erasing schemes: Constant Charge Erasing Scheme (CCES) [3] and Standard Box Erasing Scheme (SBES). Both methods are based on a sequence of N rectangular gate to bulk pulses of constant duration Δt. Their gate voltage (V_C) was kept at - 8 V. The source to bulk voltage V_{SB} has been kept at 0 V while the drains have been left floating. The other erasing parameters are summarized in Tab.I.

The voltage applied to the bulk was constant for SBES while for CCES it starts from V_B^0 and then it is increased by steps of $\Delta V_B = 0.05V$. Erasing parameters have been adjusted in order to reach the same average threshold for both CCES and SBES after erase as shown in Fig. 1. Erratic events have been measured for each cell during cycling whenever the erased threshold of the considered cell exhibits a cycle-to-cycle absolute shift larger than 250mV.

TABLE I

Sector	Δt [ms]	N	scheme	V_B^0 [V]
A	10	59	CCES	3
B	1	80	CCES	3
C	0.1	103	CCES	3
D	10	59	SBES	5.26
E	1	80	SBES	6.13
F	0.1	103	SBES	7.22
G	10	7	SBES	6.12
H	1	80	SBES	6.12
I	0.1	1000	SBES	6.12

III. Experimental Results

Fig. 1 shows that the threshold voltage distributions after erase and after programming have the same average value.

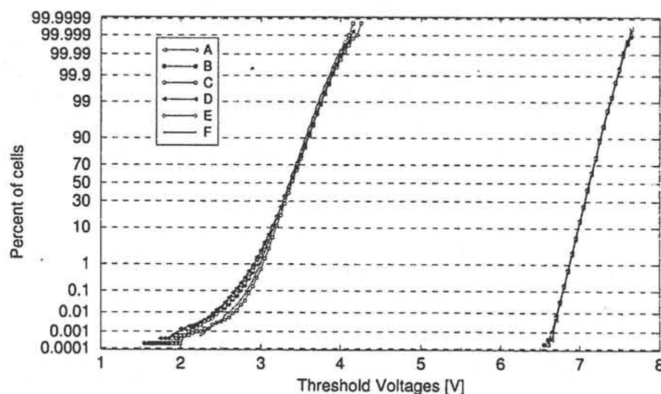

Fig. 1. Programmed and erased threshold voltage distributions of sectors A-F.

Fig. 2 shows the cumulative numbers of erratic bits marked during cycling. By comparing sectors erased with the same pulse duration but different erasing schemes it is evident that CCES drastically reduces the erratic bit failure.

On the other hand, when results obtained with the same erasing scheme are compared, from Fig. 2 it is possible to

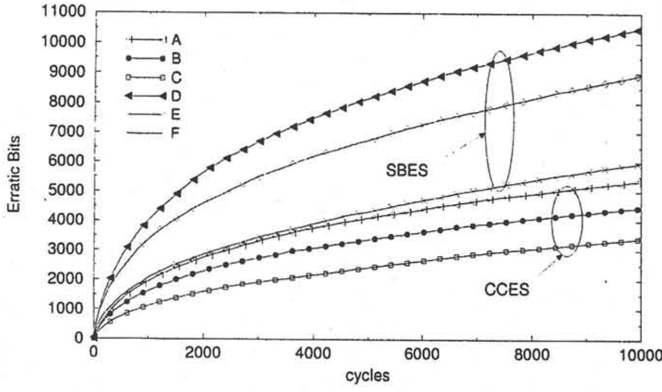

Fig. 2. Cumulative number of erratic bits detected during cycling. A bit is marked as erratic whenever it exhibits its first erratic event. Each curve belongs to different sectors (A-F).

notice that erratic bit failure of A (D) is higher than that of B,C (E,F). In order to exclude the possible influence of the electric field, we perform the same measurements on three virgin sectors G,H,I using SBES and the same bulk voltage but varying only Δt and N. As shown in Fig. 3, erratic erase increases with the pulse duration (decreases with N).

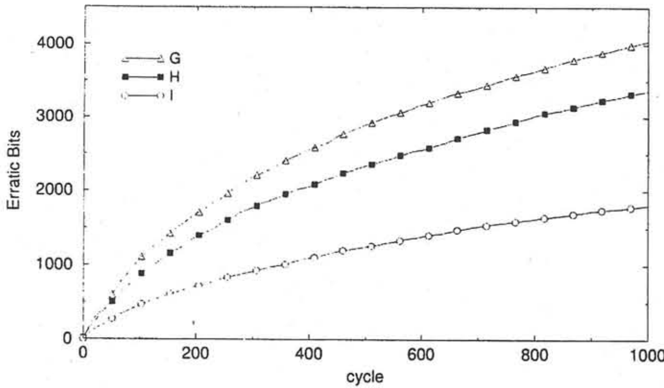

Fig. 3. Erratic bits of three sectors erased with SBES. The erased average threshold was the same, i.e. 3.42V.

Fig. 4 shows the threshold voltage shift distributions for SBES (D) and CCES (A). The dashed box evidences the larger erratic shifts exhibited by SBES with respect to CCES. SBES is therefore more prone to the leaky column risks due to erratic behaviors.

Assuming that negative shifts are caused by hole trapping and positive shifts are due to hole detrapping [4], then the cumulative difference

$$C^*(k) = C(k) - C(0) = \sum_{i=1}^{k} n(i) - p(i) \qquad (1)$$

where $n(k)$ ($p(k)$) is the number of negative (positive) shifts at cycle k, is an indicator of the hole trapping dynamics in the oxide near the floating gate. $C(0)$ is the unknown number of holes trapped in the virgin sample before cycling. Fig. 5 shows the measured $C^*(k)$ during cycling. CCES is characterized by a higher hole detrapping occurrence and $C^*(k)$ saturates reaching a minimum average value. This experimental observation evidences the presence of positive charge near the floating gate for virgin samples. SBES, on the contrary, is characterized by a higher trapping occurrence and no saturation is visible. In both cases, the higher is N (the lower is Δt), the lower is the difference between the two dynamics.

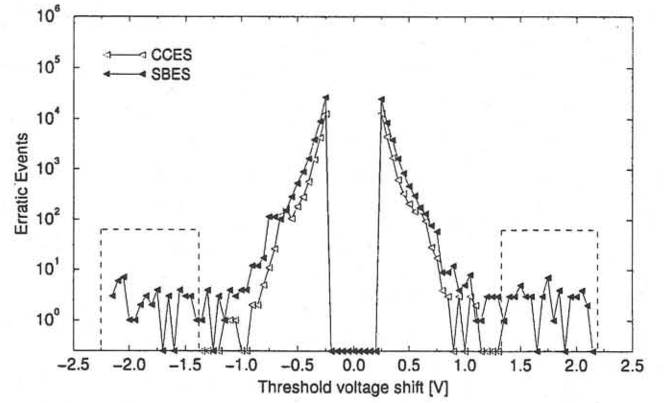

Fig. 4. Distribution of threshold voltage shifts for SBES and CCES.

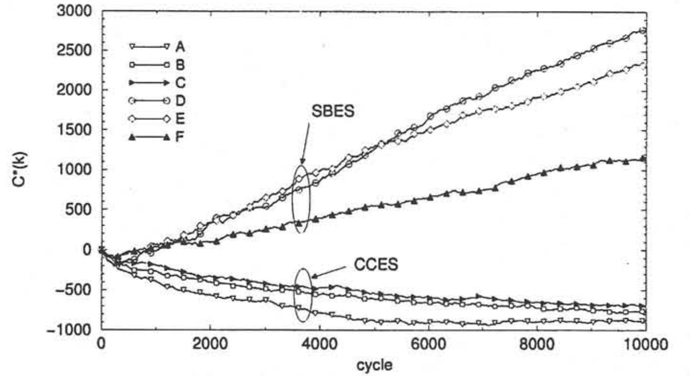

Fig. 5. $C^*(k)$ during cycling for SBES and CCES.

IV. Conclusions

It has been experimentally proven that CCES has a lower erratic erase failure rate than SBES. Other erasing parameters influencing the erratic behavior have been investigated and it has been found that erratic erase failure increases with Δt (decreases with N).

Both CCES and SBES have also been analyzed in terms of hole trapping properties. With CCES, hole detrapping is the dominant responsible erratic mechanism. On the contrary, for SBES, hole trapping has a higher occurrence. Oxide degradations due to hole trapping are therefore more dangerous for SBES than for CCES.

References

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