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Low Voltage Low Current Flash Memory Using Source Induced Band-to-Band Tunneling Hot Electron Injection to Perform Programming

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1. Introduction

Strong demands for low voltage, low power and high speed have risen in the next-generation code Flash products. The traditional channel hot electron injection programming has low injection efficiency and results in high power consumption. The Fowler-Nordheim tunneling injection, though has high injection efficiency, requires a relatively high voltage and has a slow program speed. There are several Flash cells [3][4][5] using Band-to-Band tunneling hot electron injection to realize low voltage, low current and high speed programming. However, all of these cells are based on the p-channel with read currents smaller than the half of the n-channel cells.

This paper firstly describes a novel n-channel flash memory cell with Source Induced Band-to-Band hot Electron injection (SIBE) to perform programming. Then the program characteristics and its reliability are discussed in detail.

2. Cell Structure and Technology

The proposed Flash memory cell is shown in Fig.1. A stacked gate structure, which includes a control gate and a floating gate, is firstly formed on a p-type substrate. An n-type implant is afterwards used to form the source region and a 45°-angle-tilt phosphor implant is used to form the n-halo region. A p+ region is finally formed in the n-halo region to establish the drain of the cell. The impurity concentrations of the n-halo region and the p+ region are $2\times10^{19}cm^{-3}$ and $8\times10^{19}cm^{-3}$, respectively. The tunneling oxide is 100Å and the electric thickness of the Oxide/Nitride/Oxide interpoly dielectric is 200Å. The W/L of the tested sample is 1μm/0.65μm.

3. Cell Operation and Characteristics

Program and Read

During the proposed SIBE programming operation, the source, drain and control gate voltages are set to 2.1V, -3.6V and 10V, respectively. The memory cell is turned on by the high control gate voltage and the source voltage can be transferred to the floating n-halo region. The drain p+/n junction is negatively biased, and hot electrons are induced by band-to-band tunneling in the deeply depleted p+ surface region under the gate-to-drain overlap area. A part of these hot electrons can overcome the barrier and be injected into the floating gate with the aid of V_{CG}, thereby realizing the program operation.

Though the memory cell is turned on by V_{CG}, there is a very low turn-on current due to the negative voltage drop across the series p+/n-halo diode. Fig.2 shows the leakage and programming currents as a function of the floating gate potential. The drain and floating gate currents are 2.6μA/μm and 0.8nA/μm, respectively, and the programming efficiency can reach to 3×10^{-4}. In the unselected cells contacted to the selected bit-line, because the source voltage cannot be transferred to the n-halo region, the drain leakage current and floating gate current are decreased to smaller than 1nA/μm and 1pA/μm, respectively. Therefore, the program bit-line disturbance is significantly alleviated and the bit-line leakage current is greatly reduced by using the SIBE method. Fig.3 shows the program characteristics of the fabricated cell. Threshold voltage above 4.6V is obtained within 10μs.

The negative gate source side F-N tunneling is used to perform the erase operation, during which, the drain are floated, the substrate is set to ground, and the control gate and the source are set to –10V, and 5V, respectively. Threshold voltage lower than 1V is obtained within 4ms, as shown in Fig.4.

During the read operation, V_D and V_{CG} are biased at 1.2V and 3.3V, respectively, and the other terminals are set to ground. Under this bias condition, the drain p/n-halo junction of the memory cell is positively biased and the voltage of the n-halo region is clamped at about 0.6V. With the access voltage, the p-type channel region may be inverted (in the "0" cell) so that the electrons can flow from the source to the n-halo and an access current of 64μA/μm is read out from the drain, as shown in Fig.5.

Disturbance and Endurance

During the SIBE programming, owing to the zero bias on the control gate for the disturbed cell, the source voltage cannot be transferred to the drain p+/n junction and the band-to-band hot electrons' generation and injection are depressed. The gate and drain disturb characteristics are shown in Fig.6 and Fig.7. No significant threshold voltage increment is observed during 1000 programming cycles (0.01s), suggesting that there are enough margins for both gate and drain disturbances. The endurance characteristic of 10^5 program/erase cycles is also confirmed, as shown in Fig.8.

4. Conclusion

In this paper, a novel Source Induced Band-to-Band hot Electron injection programming method is proposed and an n-channel flash memory cell is fabricated and evaluated. High program and erase speed, low program current, sufficient margin for gate and drain disturbances, large read current and excellent endurance characteristics are achieved.

Acknowledgement

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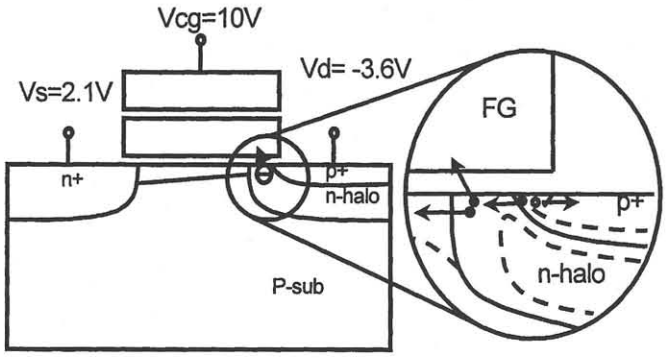

Fig.1. Cell structure and insert schematic illustration of the SIBE programming method for the n-channel cell.

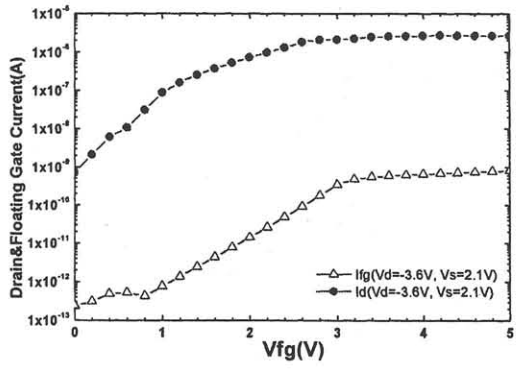

Fig2. Program currents as a function of floating gate voltage.

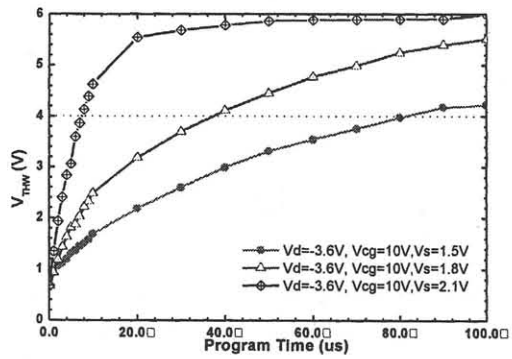

Fig3. Program characteristics.

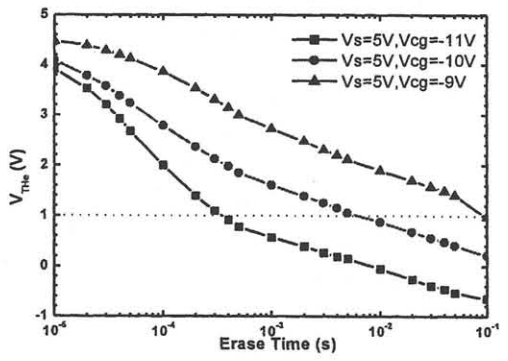

Fig4. Erase characteristics.

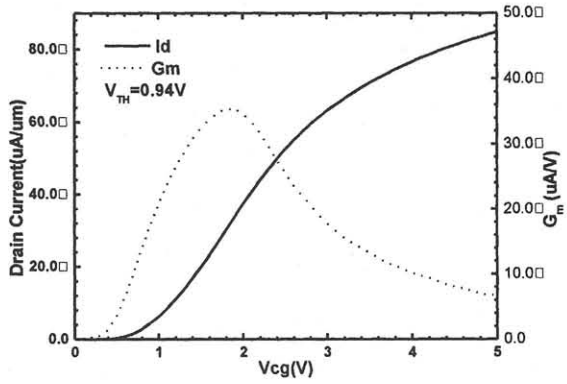

Fig5. Read characteristics.

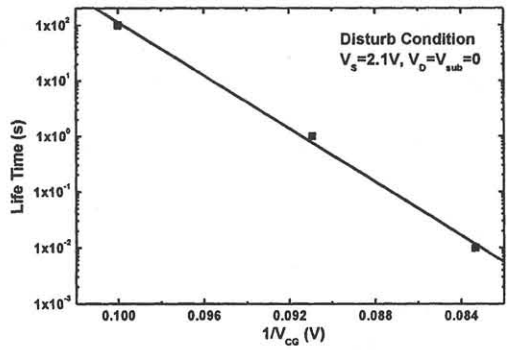

Fig6. Word-line disturb characteristics.

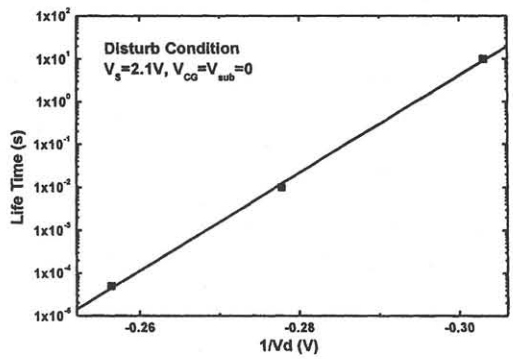

Fig7. Bit-line disturb characteristics.

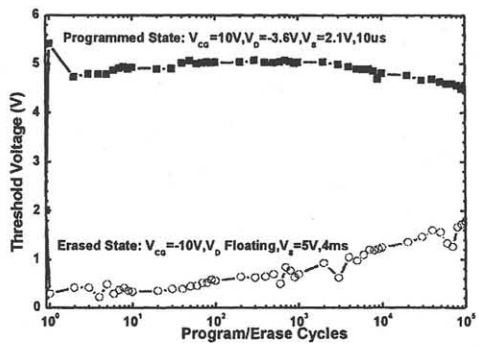

Fig8. Endurance characteristics