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Embedded MONOS Nonvolatile Semiconductor Memory Technology

Shin'ichi Minami and Yoshiaki Kamigaki[1]

Hitachi Ltd., Semiconductor & Integrated Circuits
751, Horiguchi, Hitachinaka-shi, Ibaraki 312-8504, Japan
Phone: +81-29-272-2441 Fax: +81-29-270-1792 E-mail: minami-shinichi@sic.hitachi.co.jp
[1]Kagawa Univ., Faculty of Eng., Dept. of Advanced Material Science.
2217-20 Hayashi-cho, Takamatsu-shi, Kagawa 761-0396, Japan

1. Introduction

MONOS (Metal Oxide Nitride Oxide Semiconductor) nonvolatile semiconductor memory technology has lately attracted considerable attention. The smart card micro-controller incorporating a conventional 2-Tr/bit MONOS EEPROM (Electrically Erasable and Programmable ROM) is rapidly expanding the markets for mobile applications. The MONOS transistor, with the silicon nitride dielectric having discrete charge storage, has good compatibility with advanced CMOS logic technology, and that very high reliability and yield. Then, the MONOS transistor is said to be a very promising nonvolatile memory for System on a Chip (SoC) technology. Moreover, new type of MONOS memory with hot carrier injection realizes higher density cell and higher speed programming.

2. MONOS Nonvolatile Semiconductor Memory

Conventional Tunnel Programming 2-Tr/bit Type

Conventional MONOS memory devices are erased or written by laterally uniform tunnel charge injection into the silicon nitride layer. Fig. 1 shows transmission electron micrograph of a MONOS device. We have derived trapped electrons number n_e=7×10^{18} cm^{-3} in the nitride from memory erase/write characteristics [1]. Therefore, the average distance among trapped electrons d_e is estimated as follows.

$$d_e = \sqrt[3]{\frac{1}{n_e}} = 5.2 \text{ (nm)} \qquad (1)$$

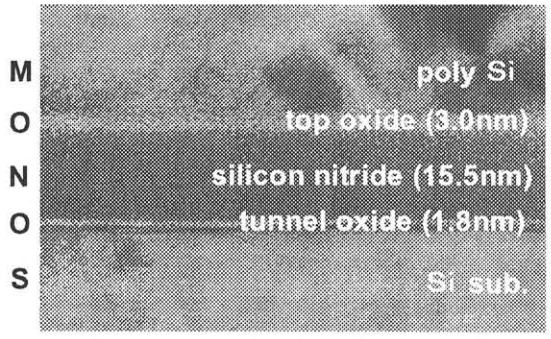


Fig. 1 Transmission electron micrograph of a MONOS structure.

The memory cell configuration is an integrated 2-Tr type consisting of a MONOS memory transistor and a select MOS transistor. We have manufactured large-scaled highly reliable MONOS EEPROM products over the last twenty years [2]. In particular, at the present time the smart card microcontroller incorporated an embedded high density 32KB/64KB MONOS EEPROM is rapidly increasing the markets for mobile applications. High-speed erase/write (1ms/1ms respectively) and 1 million-cycle endurance have been accomplished, as shown in Fig. 2. Technological breakthrough has been finding out the optimum thickness of the tunnel oxide. It might be said that we have established the conventional MONOS nonvolatile semiconductor memory technology. MONOS memory devices are suitable for the applications of logic embedded because their power consumption is lower than those of using channel hot electron injection type.

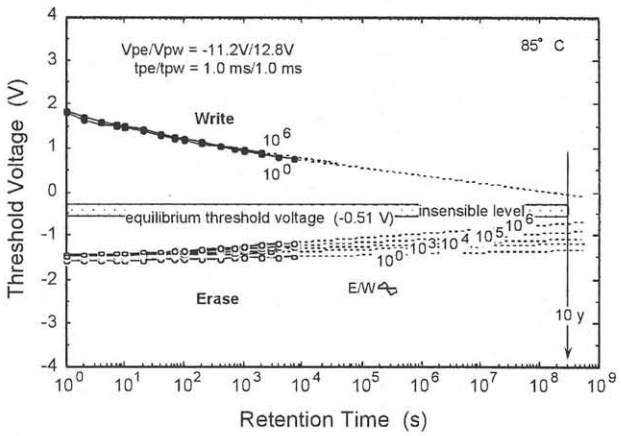
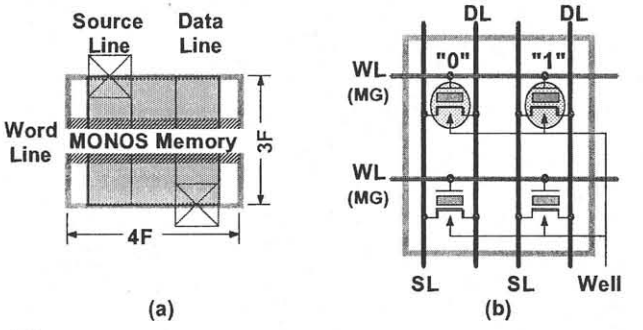


Fig. 2 MONOS retention characteristics after erase/write cycles.

Tunnel Programming 1-Tr/bit Type

A very simple one-transistor-per-bit (1-Tr/bit) memory cell has been developed [3]. This cell consists of only one self-aligned MONOS memory transistor. This cell features new bias conditions for selected and unselected cells. Figures 3(b) and (c) show the cell array circuits and the terminal voltages applied during erase, write and read, respectively. A negative voltage against the source is applied to the gates of unselected cells and the substrate

common to all memory cells with the selected gates is kept grounded. This bias condition prevents the current from flowing through unselected memory cells and the voltage from being applied to the gate insulator during read operations. The experimental and simulation results show that this new cell has no reliability problems in operation if its dimensions and structure are optimized. Although one issue for realization of EEPROMs using this new cell remains, that is, circuit design for high-speed operation with on-chip generated high or negative voltage, this new cell is very promising for full-featured high-density EEPROMs.



(c)

	WL(MG)		Selected Well			Unselected Well		
			SL	DL	Well	SL	DL	Well
Erase	Selected	$-V_p$	V_c	V_c	V_c	V_c	V_c	$-V_p$
	Unselected	Vc						
Write	Selected	Vc	$-V_p/V_c$	$-V_p/V_c$	$-V_p$	V_c	V_c	$-V_p$
	Unselected	$-V_p$						
Read	Selected	Vc	Vc	V_d	0	V_c	F	0
	Unselected	0						

WL(MG): Word Line (Memory Gate), SL: Source Line, DL: Data Line, $-V_p'$/ V_c : "0"/ "1" programming, Programming voltage $-V_p = -V_p' - V_c$, V_c: Power voltage, $-V_p'$: Generated voltage, V_d~ V_c+1V, F: float.

Fig. 3 1-Tr/bit type MONOS cell and operation

Hot-Carrier Programming 2-bit/Tr Type

A novel single-transistor MONOS EEPROM device NROM has been proposed [4]. The cell stores two physically separated bits at both edges oh the MONOS transistors. This memory is programmed by drain side channel hot-electron injection (CHE) and erased by hot hole enhanced tunneling. By local hot carrier injection into spatially discrete charge trapping centers in nitride films, 2bit multi-storage memory cell has been realized.

The programming current of NROM is relatively high. To improve programming efficiency, new 2-bit/Tr type MONOS cell with assist gates has been proposed (Fig. 4) [5]. With source side injection, program current can be reduced to less than 1 uA. Byte erase function is also possible.

Same promising ideas for utilizing an MONOS type memory device with local hot carrier injection have been proposed, such as above mentioned two examples and others.

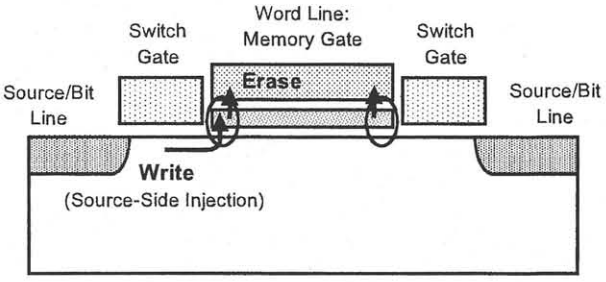


Fig. 4 Source side injection type 2-bit/Tr MONOS memory cell

Technology Comparison

Three MONOS memory cell technologies have been compared in Table I. Conventional 2-Tr/bit MONOS is suitable for the smart card application or embedded data memory. 2-Tr/bit MONOS is rather for the flash memory application or embedded program memory. 1-Tr/bit MONOS is moderate solution.

Table I Cell technology comparison

Parameter	*2-Tr/bit*	*1-Tr/bit*	*2-bit/Tr*
Bit size	20 F^2	12 F^2	4 F^2
Min. erase unit	Byte	Byte	Byte
Endurance	10^6	10^6	10^4
Program time	1 ms	1 ms	1 us
Program current	1 pA	1 pA	0.1 uA
Erase time	1 ms	1 ms	10 ms
Erase current	1 pA	1 pA	1 pA
Read-out current	15 uA	10 uA	10 uA

3. Conclusions

We have manufactured large-scaled highly reliable MONOS EEPROM products for the past twenty years. As a result, it might be said that Hitachi has established the conventional MONOS nonvolatile semiconductor memory technology. We are convinced that MONOS technology will continue to advance into mobile application areas as one of the most promising nonvolatile memory devices.

References

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