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A Novel Structure of SiO_2/SiN/High k Dielectrics, Al_2O_3 for SONOS Type Flash Memory

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1. Introduction

The NROM devices using a localized trapping in SiN show high speed and good data retention [1]. However, this device is not suitable for mass data storage beyond gigabit like NAND flash memories because of a great amount of power consumption generated by the hot carrier program/erase operation. In contrast, the SONOS programmed and erased by Fowler-Nordheim (FN) tunneling, especially the NAND-type SONOS, is more compatible with mass storage application in view of power consumption and scalability. In the NAND-type SONOS, since the erase speed is determined by the competition of the direct band-to-band (DT) tunneling current through a tunnel oxide and the unwanted FN tunneling current through a blocking oxide, the tunnel oxide thickness is fundamentally required to be less than 20Å for a stable erase operation [2]. Accordingly, the considerable charge loss of the SONOS due to DT tunneling through the very thin tunnel oxide is an obstacle for the SONOS to be applied as a commercial flash memory in spite of its superior scalability and endurance characteristics over the floating gate memories as shown in table 1.

In this paper, we propose a new SONOS device structure that can make fast program/erase operation by FN tunneling mechanism possible even at a thicker tunnel oxide over 30Å. This is achieved by employing a high-k dielectric material, Al_2O_3 replacing the top silicon oxide for a blocking layer as illustrated in Fig.1. Furthermore, this structure achieves long data retention and realizes low voltage programming.

2. Simulation for Device Design

We simulated the SONOS devices to investigate the effect of high-k dielectrics as a blocking layer on the erase characteristics. The charge trapping phenomena in SiN are modeled to be governed by a hole current through a tunnel oxide (J_h in Fig. 2) and an electron current through a blocking layer (J_e) in this simulation [3].

The simulated erase characteristics of conventional SONOS device as a function of a tunnel oxide thickness are shown in Fig. 3. It is found that the entire electrons charged in SiN are removed from the trap of SiN by the erase operation in 20Å-thick tunnel oxide. However, in the case of tunnel oxide thickness exceeding over 25 Å, erased threshold voltage (V_{TH}) is saturated at the higher level.

In order to suppress the gate injection current as mentioned above, we introduce high k dielectric into a blocking layer. Using high-k dielectric material for the blocking layer, the electric field across the tunnel oxide can be increased, while that across the blocking oxide is reduced as shown in Fig. 2. As the dielectric constant of a blocking layer increases, the difference of the hole current (J_h in Fig. 2) and the electron current (J_e) becomes larger under erase operation and thus the erase voltage is reduced as well as program voltage. To be used as a blocking layer of SONOS devices, the high-k dielectric characteristics requires to have larger bandgap for the bake retention and larger take-off voltage for the suppressed gate injection. Al_2O_3 shows higher turn-on voltage from 3 MV/cm to 6 MV/cm with the energy bandgap of 8.9eV (inset of Fig. 4). We named this device as SANOS (Silicon-Aluminum-Oxide-Nitride-Oxide-Silicon, SiO_2/SiN/Al_2O_3). Fig. 4 shows the simulated erase characteristics of a SANOS device with SiO_2/SiN/high-k dielectrics, Al_2O_3. The saturation of erase threshold voltage is not observed in 30Å-thick tunnel oxide. The erase voltage is increased, the erase speed is increased and the erase threshold is decreased. From these simulation results, we show the device structure of SiO_2/SiN/high-k dielectrics enables an erase operation by FN tunneling mechanism through a thicker tunnel oxide exceeding to DT tunneling regime as well as the feasibility of Al_2O_3 as a blocking layer of SONOS devices.

3. Experimental Results

The TEM of SANOS is shown in Fig. 5. Al_2O_3 was prepared by atomic layer deposition (ALD) using Trimethylaluminum (TMA), $Al(CH_3)_3$, and H_2O and showed the dielectric constant of 8 and the turn-on field of 3MV/cm [2].

Fig. 6 shows the program and erase speed characteristics of SANOS device with 30Å-thick tunnel oxide. As the erase voltage increases up to 18V, the saturation level of erased V_{TH} has been lowered and erase time is lowered to 10ms with 5V threshold voltage (V_{TH}) shift. In the conventional SONOS device with less than 20Å tunnel oxide, the erased V_{TH} is formed at the lower level than the initial one due to easy hole trapping in SiN, while the erased V_{TH} is saturated at the higher level in SANOS device. However, the electron injection from the gate is not observed even at the larger erase voltage up to 18V. It can be concluded that the electron injection is suppressed by high-k dielectric, Al_2O_3. The leakage current characteristics of the Al_2O_3 layer are sufficient to block the electron injection from the gate in the reasonable erase voltage range. These good erase characteristics are kept in 40Å-thick tunnel oxide (Fig. 7). Larger electric field in tunnel oxide than the 30Å-thick tunnel oxide is required to achieve the same V_{TH} shift as the 30Å-thick tunnel oxide owing to the significant reduction of direct tunneling current. Therefore, the tunnel oxide thickness would be optimized in view of program/erase speed and bake retention. Fig. 8 shows the bake retention characteristics of the SANOS device with 30Å-thick tunnel oxide. After 2hrs bake at 250°C, there was V_{TH} shift of 0.7V, which is a comparable value to that of floating gate devices. We believe that the excellent data retention characteristics could be achieved by using a thicker (>20Å) tunnel oxide and thus suppressing the electron discharging due to DT tunneling mechanism. The reliability of these SANOS devices will be reported elsewhere.

4. Conclusion

We have developed a new device structure of SiO_2/SiN/high-k dielectrics for the NAND-type SONOS with high density and better data retention. The effect of replacing the top blocking oxide into high-k dielectric material, Al_2O_3 on the erase characteristics of SONOS devices is investigated. Even the tunnel oxide thicker than 30Å is used, the SANOS device shows faster erase speed and larger erase V_{TH} shift than the conventional SONOS device. Moreover, we observed that Al_2O_3 is feasible to block the gate injection current under higher erase voltage and loss of charge stored in SiN.

References

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[2] J. Bu and M. H. White, Solid State Electron. **45**, 113 (2001)
[3] F. R. Libsch and M. H. White, Solid State Electron. **33**, 105 (1990)

	NROM	NAND Floating Gate	NAND SONOS	NAND SANOS
Bit size	$2.5F^2$ (MLC)	$4.6F^2$	$4F^2$	$4F^2$
Minimum device size	0.17 μm [1)]	0.12 μm [2)]	0.12 μm	0.12 μm
Product	512Mbit (MLC)	1Gbit (SLC)	Not reported	Not reported
PGM/ERS method	channel hot electron/hole	FN tunneling	FN tunneling	FN tunneling
Endurance	Good	Severe	Good	Not reported
Bake retention	Good	Good	Bad	Good
Scalability to 0.1 μm below	Difficult	Very Difficult	Easy	Easy
Technology maturity	New	Very High	New	New

Table 1. Comparison of NROM, NAND floating gate, NAND SONOS and NAND SANOS technology ([1), 2)] most advanced cell being reported).

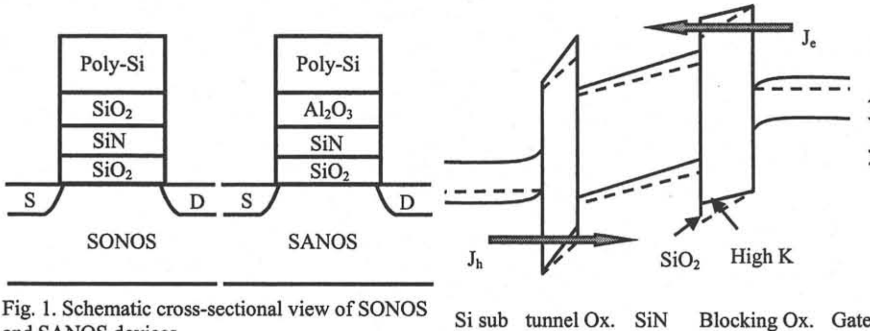

Fig. 1. Schematic cross-sectional view of SONOS and SANOS devices.

Fig. 2. Energy band diagram of the SONOS (---) and the SANOS (—) devices at the erase mode.

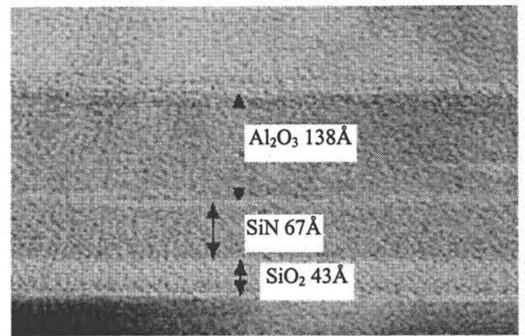

Fig. 5. Cross sectional TEM image of SANOS device (43Å SiO_2/67Å SiN/138Å Al_2O_3).

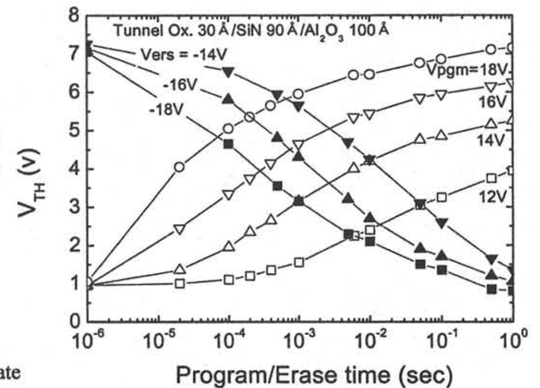

Fig. 6. Program and erase characteristics of SANOS device with 30Å tunnel oxide, 90Å SiN, 100Å Al_2O_3 (PMOSFET with W/L=12.4μm/0.27μm).

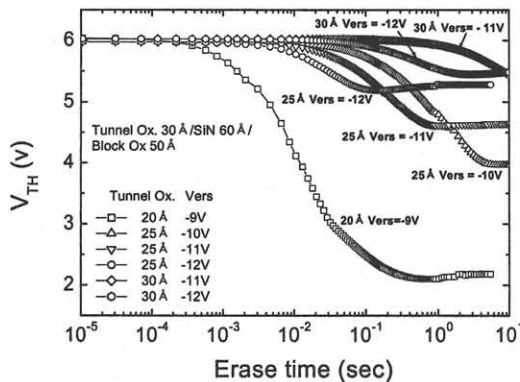

Fig. 3. The simulated erase characteristics of SONOS devices as a function of tunnel oxide thickness (20Å, 25Å, 30Å). ($V_{TH_INITIAL}$=2V, V_{TH_PGM}=6V, hole mobility=0.7m_0, electron mobilty=0.55m_0).

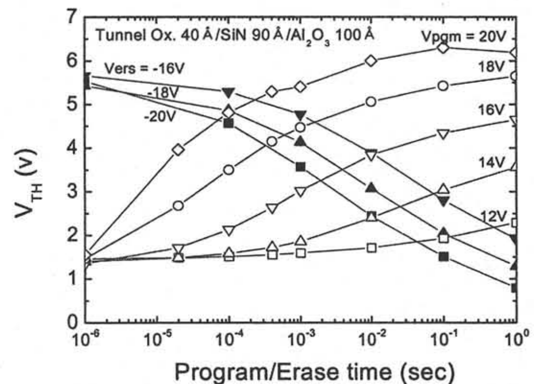

Fig. 7. Program and erase characteristics of SANOS device (SiO_2/SiN/Al_2O_3) with 40Å tunnel oxide, 90Å SiN, 100Å Al_2O_3 (PMOSFET with W/L=12.4μm/0.27μm).

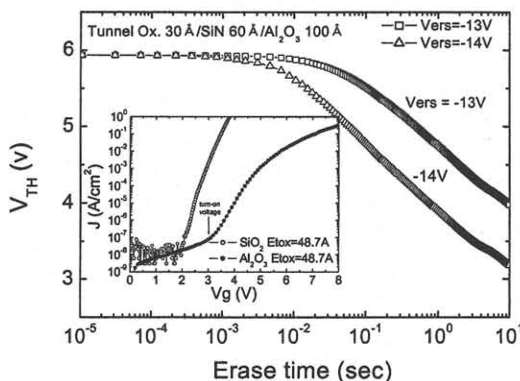

Fig. 4. The simulated erase characteristics of SANOS devices (SiO_2/SiN/Al_2O_3) with tunnel oxide thickness of 30Å (dielectric constant of Al_2O_3 =8.0, $V_{TH_INITIAL}$=2V, V_{TH_PGM}=6V, hole mobility=0.7m_0, electron mobilty=0.55m_0).

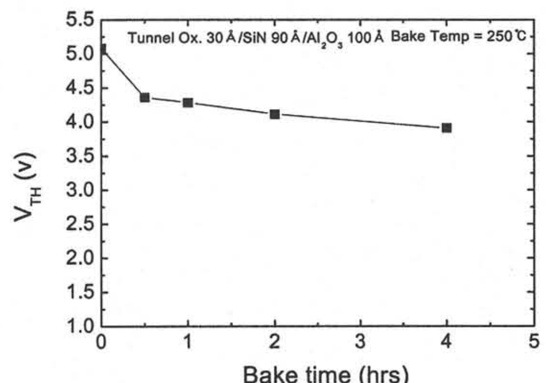

Fig. 8. Data rentention characteristics of the fresh SANOS device (SiO_2/SiN/Al_2O_3) with 30Å tunnel oxide, 90Å SiN, 100Å Al_2O_3 at 250°C.