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# Hot Carrier Enhanced Read Disturb and Scaling Effects in a Localized Trapping Storage SONOS Type Flash Memory Cell

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## 1. Abstract

Read disturb induced threshold voltage (Vt) instability in a localized trapping storage flash memory cell with a SONOS type structure is investigated and reported for the first time. Our results show that positive oxide charges created during P/E stress is the cause of Vt shift. Both gate voltage and drain voltage will accelerate this Vt drift. Hot carrier enhanced degradation is severe in a scaled device, especially at low temperature.

## 2. Introduction

Recently, localized trapping storage, two bit per cell flash memory technology by using hot electron programming and hot hole erasing (NROM [1] and MXVAND [2], Fig.1) has attracted much attention for its smaller cell size, simpler fabrication process, no drain induced turn-on and better cycling endurance [1-4]. Data retention characteristics of this cell have been discussed [2, 5-6]. Though sufficiently high Vd is necessary for reverse read operation [1], read disturb is rarely explored. Fig.2 shows the observed Vt shift of a P/E cycled cell. The applied gate and drain biases are the same as read operation. This Vt shift will degrade memory window and result in the memory cell malfunction. The purpose of this work is to find the dominant mechanisms that cause the Vt instability.

## 3. Experimental

The samples used in this work are made of an n-channel MOSFET with an oxide-nitride-oxide (ONO) gate dielectric structure. The thickness of each ONO layer is 9nm (top oxide), 6nm and 7nm. Devices with gate length from 0.5μm to 0.3μm are characterized. Temperature effect from –20C to 85C is studied. Two disturb modes are investigated for P/E cycled cells in erase state. One is with applied gate and drain biases and the source is grounded. It is the conventional read disturb (RD) mode. The other is with an applied gate bias and the source and drain are grounded. It is termed as room temperature drift (RT) mode since the Vt drift is independent of temperature at such bias scheme [7]. It is to emulate the gate disturb effect on the cells belonging to the same wordline of the selected cell.

## 4. Results and Discussions

*Read disturb model*

Fig.3 shows the Vt shift of a 10K P/E cycled cell in a two-phase measurement, e.g. RT and RD are measured in sequence, or vice versa. It is found that after RT (or RD), the subsequent RD (or RT) is reduced. This implies that RT and RD are not caused by independent mechanisms since they influence each other. It also means that Vt shift due to RD is dependent on the sampled time. Since positive oxide charge detrapping (with the co-existence of residual negative charges in nitride) is clarified to be the major cause of RT [2], these positive oxide charges created during P/E cycling are suspected to affect RD. Fig.4 (a)-(c) illustrate the Vt drift models at various bias conditions. Both positive oxide charge tunnel detrapping and positive charge-assisted electron tunneling (PCAT) will result in the positive Vt shift. Based on the study in [8, 9], the corresponding Vt temporal evolution is modeled as shown in Table 1.

*Bias dependence of read disturb*

Fig.5 shows the RT characteristics of a 10K P/E cycled cell. The applied gate bias is from Vg=0V to Vg=4V. We plot the Vt drift versus applied gate bias in Fig.6. It is found that Vt shift shows linear dependence on log(t) for Vg=0V and 3V. This has been well modeled by hole tunnel detrapping [8] (Fig.4 (a)). However, accelerated Vt drift, which exhibits power law time dependence $t^n$, is observed at Vg=4V. It has been reported that PCAT has power law time dependence ($J_{cat} \propto t^{-p}$, Table.1 [9]). Accordingly, the time evolution of Vt drift would show power law time dependence $t^n$, where n=1-p, if PCAT dominates. The accelerated Vt drift with its unique time dependence confirms that positive charge-assisted electron tunneling to the trapping nitride (Fig.4 (b)) takes place at high vertical field, in addition to hole tunnel detrapping.

Fig.7 shows the RD characteristics of a 10K P/E stress cell with Lg=0.5μm. The drain bias is from 1.7V to 2.3V and the gate bias is 3V. Vt shift versus drain bias is shown in Fig.8. Since the nitride conduction band edge is 2.1eV above the silicon conduction band edge, sufficient lateral field heating is necessary to make the channel electrons inject into the trapping nitride, if the vertical field is low. Unlike Vg-accelerated RT, the dramatically enhanced RD found at high drain bias (Vd=2.3V) can be explained by the hot carrier effect (Fig.4 (c)). In addition, the $t^n$ time dependence of Vt drift also indicates that PCAT process is involved. As Vd decreases, hot carrier effect is too weak to make the electrons inject into the trapping nitride. The Vt shift is then dominated by hole tunnel detrapping. It is the same as RT (Fig.4 (a)). Furthermore, reduced Vt shift at Vg/Vd=3V/1.7V than that at 3V/0V can be explained by reduced vertical field in the former case.

Vd acceleration is widely used for hot carrier lifetime projection. As shown in Fig.9, Vd acceleration effect is observed at high Vd. However, gate enhanced read disturb, instead, dominates at low drain bias where hot carrier effect is insignificant. Vt shift is almost independent of Vd in this regime (e.g. Vd<2V with Lg=0.5μm). The extrapolated lifetime based on the results at high Vd regime will be overestimated if we use a low drain voltage during read operation, where hot carrier effect is very weak.

*Channel length scaling effect*

It is known that hot carrier effect will be detrimental in a scaled device. Fig.10 shows the RD results of three cells with Lg=0.5μm, 0.4μm, and 0.3μm, respectively. Increased RD is observed in a short channel device. In addition, Vt shift temporal evolution exhibits $t^n$ time dependence for Lg=0.3μm. It implies that strong hot carrier enhanced RD dominates Vt shift as channel length is scaled down.

We also investigate the temperature effect on RD. Hot carrier theory concludes that high energetic carriers decrease at high temperature due to increased phonon scattering. Fig.11 shows that RD is almost independent of temperature in a long channel device (Lg=0.5um), since hole tunnel detrapping dominates. On the other hand, enhanced RD is observed at low temperature in a scaled device (Lg=0.3um), where hot carrier enhanced degradation dominates.

## 5. Conclusions

Read disturb induced Vt instability is investigated in this work. It is found that gate voltage enhanced Vt drift occurs in long channel device. Hot carrier effect (drain field heating) dominates the enhanced Vt shift in a short channel device, especially at low temperature. Both are related to positive oxide charges created during P/E stress.

**Acknowledgements**

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Table 1. Vt instability model

| | |
|---|---|
| hole tunnel detrapping | |
| $J_h \propto \frac{N_h}{\sqrt{m_h \phi_h}} t^{-1}$ | $\Delta V_t^{\,h}(t) \propto \frac{N_h}{\sqrt{m_h \phi_h}} \log(t)$ |
| positive charge-assisted electron tunneling | |
| $J_{cat} \propto N_h t^{-p}$ | $\Delta V_t^{\,cat}(t) \propto N_h t^{n}$ |
| $p \propto \sqrt{\frac{m_e \phi_e}{m_h \phi_h}}$ | $n = 1 - p$ |

$N_h$ denotes the volumetric positive oxide charge density.
$m_e$ and $m_h$ are the electron and hole effective masses, respectively.
$\phi_e$ and $\phi_h$ are trapped hole and electron tunneling barrier heights, respectively.

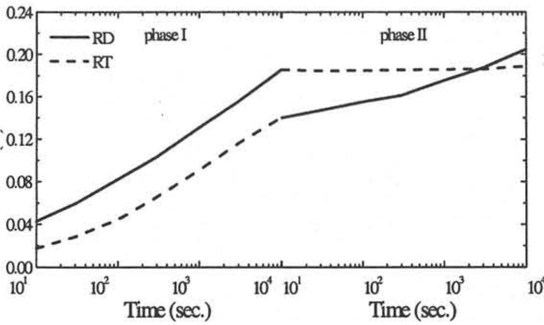



Fig.3 Two-phase measurement of the Vt shift versus disturb time of a 10K P/E cycled cell. Successive RT and RD, or vice versa, are monitored. Bias conditions of RT and RD are Vg/Vd/Vs=0V/0V/0V and Vg/Vd/Vs=3V/1.6V/0V, respectively. Lg=0.5μm.

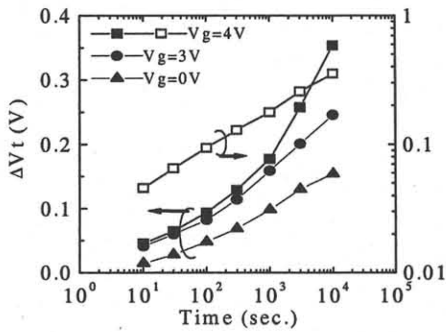



Fig.5 Vt shift versus disturb time of a 10K P/E cycled cell at various applied gate biases. The drain and source are grounded. Lg=0.5μm.

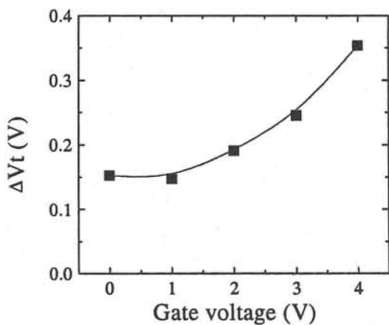



Fig.6 Vt shift versus applied gate bias of a 10K P/E cycled cell. The drain and source are grounded., and the disturb time is 10000 sec. Lg=0.5μm.

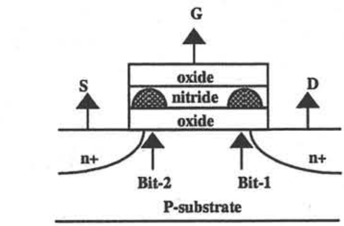



Fig.1 Schematic representation of the cell structure and localized charge storage.

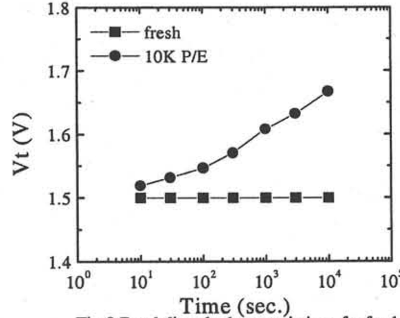



Fig.2 Read disturb characteristics of a fresh cell and a 10K P/E cycled cell. Lg=0.5μm.

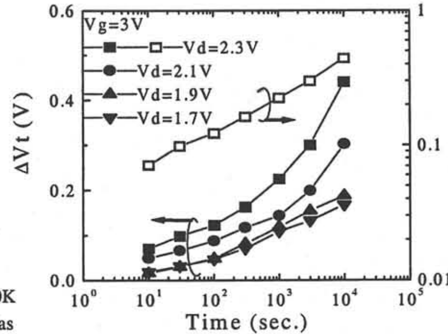



Fig.7 Vt shift versus disturb time of a 10K P/E cycled cell at various drain biases. Lg=0.5μm.

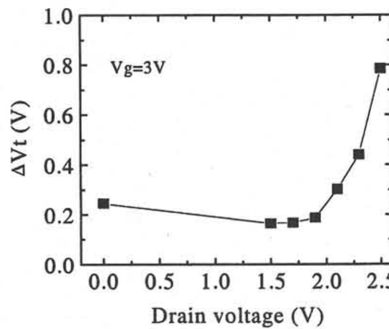



Fig.8 Read disturb induced Vt shift versus applied drain bias of a 10K P/E cycled cell. The disturb time is 10000 sec. Lg=0.5μm.

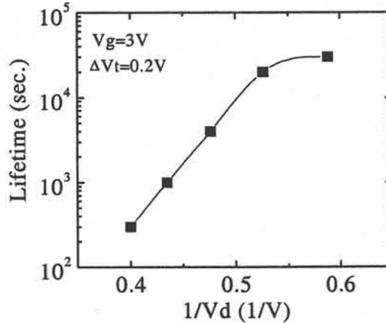
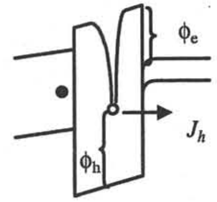
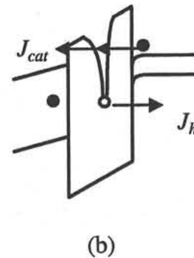


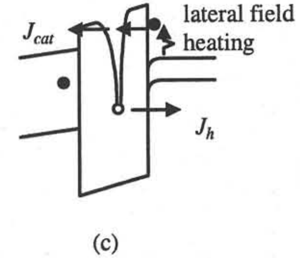

Fig.9 Lifetime projection by Vd acceleration approach. Lifetime is defined as the disturb time sustained for a 0.2V Vt shift. Lg=0.5μm.




(a)




(b)




(c)

Fig.4 Schematics of band diagrams and carrier transport mechanisms at various bias conditions. $\phi_h$ and $\phi_e$ represent the hole and electron tunneling barrier heights, respectively. Three carrier transport paths are illustrated: (a) Positive oxide charge tunnel detrapping at low oxide field ($J_h$). (b) Positive oxide charge-assisted electron injection into nitride ($J_{cat}$), in addition to $J_h$, at high oxide field. (c) Positive oxide charge-assisted electron injection into nitride ($J_{cat}$), in addition to $J_h$, at high lateral field. Hot carriers are generated due to lateral field heating.

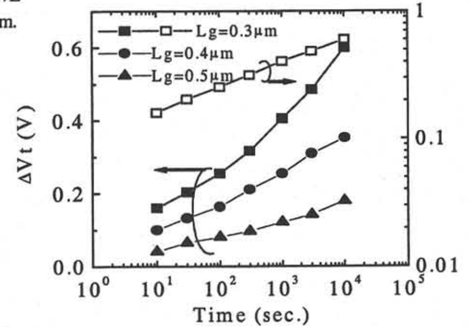



Fig.10 Vt shift versus disturb time of 1K P/E cycled cells with different channel lengths.

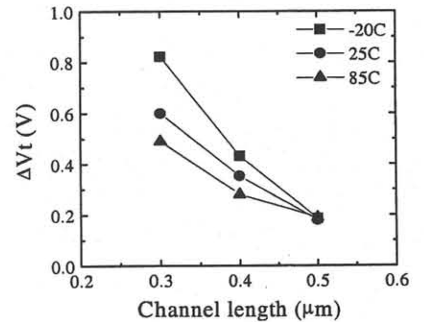



Fig.11 Temperature effect on read disturb of 1K P/E cycled cells. Devices with gate length of 0.5μm, 0.4μm and 0.3μm are characterized. The applied gate and drain biases are 3V and 1.6V, respectively, and the disturb time is 10000 sec.