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Characterization of *micro*FLASH® Memory using "Dummy" GOX Structures

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1. Introduction

The *micro*FLASH® technology employs n-channel memory transistors with an ONO dielectric. Programming is performed by channel hot electrons (CHE) and erase by holes generated in the drain region by band to band (BBT) tunneling and then accelerated in the lateral field. The read operation is in the direction opposite to programming. Two memory bits are located at opposite channel edges of one transistor (NROM™ concept[1]).

Direct measurements of gate electron and hole currents (I_e, I_h) are very helpful for optimization of memory transistors. In transistors with an ONO dielectric, I_e and I_h decay rapidly and their monitoring is very complicated. The idea of this paper is to substitute the ONO stack in actual memory cells with GOX of the same equivalent thickness. This allows the control of electron and hole currents in regimes close to real operation conditions of *micro*FLASH. In addition to current measurements, "dummy" GOX structures allow one to distinguish between the effects connected with in-process charging of ONO and the statistical spread of Vt originating from photolithography and implantation limitations. This paper is intended to illustrate the application of "dummy" GOX methodology in *micro*Flash engineering.

2. Comparison of ONO and "dummy GOX" structures

The studied specimens were processed in a standard *micro*FLASH process flow. After forming the memory cell (array), the ONO was etched off and substituted with thermal GOX of the same thickness. The cell geometry and drain doping profiles were the same as in real *micro*FLASH transistors.

$I_d(V_g)$ characteristics of real *micro*FLASH cells and C-V characteristics of ONO and "dummy" GOX capacitors are compared in Fig.1. The characteristics are identical but shifted along the Vg axis. The Vt difference of ~ 0.4-0.6 V is due to negative charge trapped in the ONO. Higher shifts for transistors compared with capacitors is an edge effect connected with in-process UV charging of the ONO. UV charging is more pronounced in narrow ONO single cells. Statistical results for mini arrays are presented in Fig.2. These results are consistent with measurements of 2Mb arrays. The results indicate an approximately 50% decrease in Vt spread for 'dummy" arrays.

3. Injection currents

Fig.3 shows the gate currents in "dummy" GOX cells in different operation conditions. The first peak (negative current) is connected with hot holes injected at the drain edge. The second peak is connected with CHE injection. The increase of Ig for voltages above 10V is due to F-N injection in the source region. The value of the hole current in a typical *micro*Flash erase regime (Vg=0, Vd=8V, Vs=3V) can be found in Fig.4. The graph allows one to estimate the erase time τ_e. Values of ~ 20ms are consistent with measurements of real cells with an ONO dielectric. The Vg that is used in real ONO cells for programming is somewhat higher than Ig peak value. This is due to the trade-off with the bulk current, Ib. Avalanche holes generate secondary electrons that can be trapped far from the drain. It is clear that it is difficult to erase the charge trapped far from the junction by BBT holes. The increase of Vg to ~9V still allows programming times of the order of few microseconds.

3. Simulation of Bit 2 influence

The endurance performance of microFlash cells strongly depends on the state of Bit 2 in the case of Bit 1 cycling. This was shown to be related to trapping far from the drain edge. By using an aggressive CHE regime it was possible to create traps in GOX from one side of the "dummy GOX" transistor channel. The degraded side of the "dummy" cell was programmed/erased in a standard *micro*FLASH regime (Fig.5). Thus, measurements of currents in conditions simulating programmed Bit 2 could be fulfilled. Vd for programming Bit 1 with programmed Bit 2 was ~0.5 V higher. Substrate currents strongly decreased when the source side of the transistor (Bit 2) was programmed. This is illustrated by Fig.6a (Ib before and after programming Bit 2) and by Fig.6a (after Bit 2 erase). The obtained results imply that part of primary CHE are also trapped far from the drain. Special drain engineering was done to decrease the amount of electrons trapped far from drain. Together with proper selection of operation conditions this allowed over 100k cycling endurance of *micro*Flash products to be achieved [2,3].

4. Conclusion

We have shown the effectiveness of 'dummy" GOX methodology in the engineering of *micro*FLASH memory. Measurements of "dummy" cells allow the selection of the proper programming/erase conditions and the optimization of the technology in order to increase endurance.

5. References

[1] B.Eitan, *US Patent* 5,768,192, June 16, 1998.
[2] E.Aloni, et al , SSDM 2000 (Sendai), p.298
[3] Y. Roizin, et al, IEEE NVSM Workshop (2001, Monterey, CA), p.128.

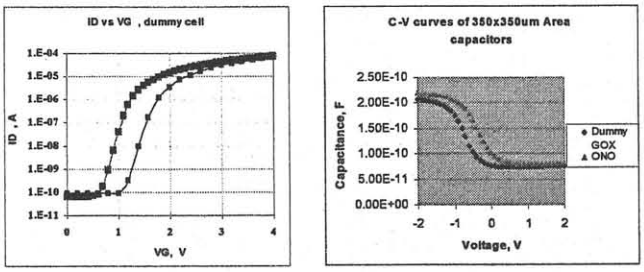


Fig.1 Comparison of Vt for "dummy cells and *micro*FLASH with ONO (L_{eff}=0.32um, W=0.35um, effective ONO thickness ~190A)

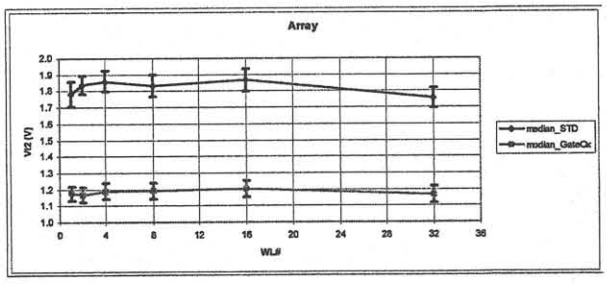


Fig.2 Vt distributions for microFLASH (ONO) and dummy Arrays. X-axis is the number of the word line.

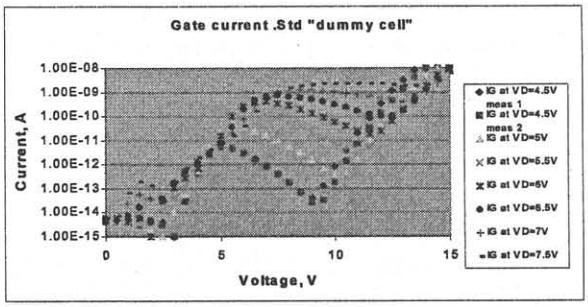
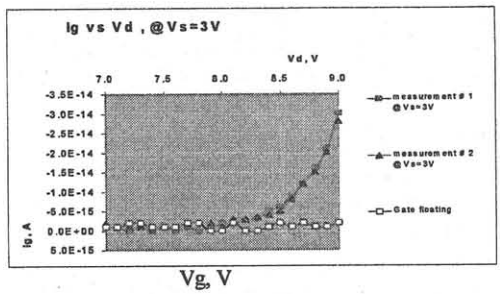


Fig.3 Gate current in the "dummy" GOX cell



Vg, V

Fig.4 Hole gate current in "dummy" cells as a function of Vd. Vg=0V and Vs=3V . simulating the erase regime of *micro*FLASH

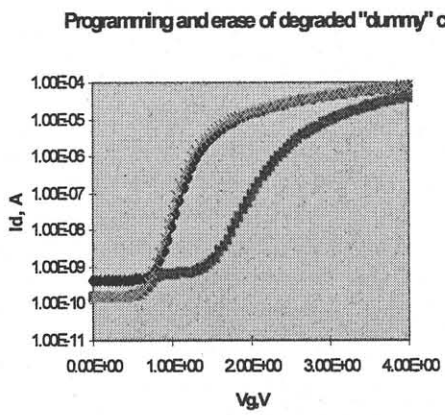


Fig.5 Programming of the "dummy" GOX cell
The GOX was degraded by Vg=10V, Vd=6V pulses from one side of the channel. Charge was written and erased from this damaged region

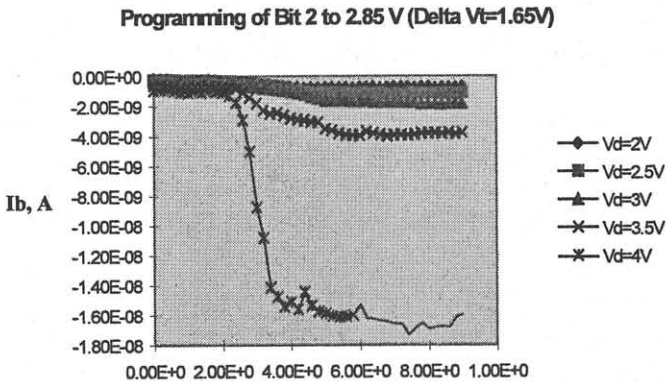


Fig.6a Substrate currents of "dummy" cell measured for different Vd after programming of Bit 2. Vt before programming was 1.115V.

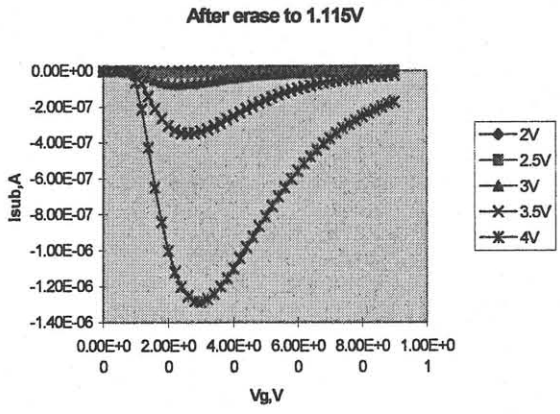


Fig.6b Substrate currents of "dummy" cell measured after erase of Bit 2. Vt to the initial Vt. Bulk currents returned to their values before degradation of Bit 2 region and programming it.