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# Modified Gate Re-oxidation Technology for High Performance Embedded DRAM by Self-Adjusted Gate Bird's Beak

Y. Nishida, S. Ueno, T.Uchida,T. Terauchi, T. Tsunomura, M.Takeuchi, M. Shirahata, T. Eimori and Y. Inoue
*ULSI Development Center, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, Hyogo 664-8641, Japan*
Telephone: +81-727-84-7322, Fax: +81-727-80-2693, e-mail: ynishida@lsi.melco.co.jp

## 1.Introduction

Development of System-on-a-chip (SoC) technology is a very important theme for recent semiconductor industry, and embedded DRAM (eDRAM) is one of the main products of SoC. As systems become more sophisticated and their transistors become smaller, it becomes more difficult to find a simple process solution which achieves the best performances for all components in SoC [1]. For example, logic components in eDRAM need high-speed ability, which means that thin gate insulator thickness ($T_{OX}$) is necessary to realize high drain current ($I_D$). On the other hand, in order to maintain high reliability at high electric field, DRAM cell transistors need thick $T_{OX}$ with gate bird's beak by gate re-oxidation after gate electrode formation. Gate bird's beak thickens the gate insulator near gate edge and rounds the gate electrode corner, and reduces gate-induced drain leakage (GIDL) [2]. However, large gate bird's beak by re-oxidation for thick $T_{OX}$ transistors has bad influence upon the thin $T_{OX}$ transistors.

In this paper, we propose a new simple process, that is, modified gate re-oxidation method. The modified gate re-oxidation method self-adjusts the amount of gate bird's beak according to gate width ($W_G$). This method effectively makes large gate bird's beak for DRAM narrow $W_G$ memory cell region where GIDL suppression is very important, and also makes small gate bird's beak for random logic region where high $I_D$ drivability is very important. As a result, this modified gate re-oxidation process realizes the ideal embedded DRAM which has both high reliable memory region and high-speed logic region.

## 2.Device Fabrication

Schematic images of gate re-oxidation are shown in Fig.1. Figure (a) shows the case of conventional gate re-oxidation and (b) shows that of the modified one. Figure 2 shows SEM images of modified gate re-oxidation process. Figure (a) is before the oxidation, and (b) is after the oxidation. Figure 3 shows two process sequences, conventional one and modified one. After formation of trench isolation, well and channel, gate insulator is formed by dual oxidation process. Then, Poly-Si layer is deposited and gate electrode is patterned. Here, in the conventional process, gate bird's beak is formed by rapid thermal oxidation (RTO). Then, Lightly doped drain (LDD) layer is made and gate sidewall spacer is formed with $Si_3N_4$. Here, in the modified gate re-oxidation process, furnace oxidation (FO) is performed. By this operation, bird's beak grows under the $Si_3N_4$ spacer and reaches the gate electrode edge. This is the same phenomenon as local oxidation of silicon (LOCOS) process [3]. Consequently, the gate edges become thick as shown in Fig.1 and Fig.2 (b). The following processes, deep source / drain layer formation and so on, are the same as the conventional ones. In this experiment, we made some samples with different FO time. The conventional gate re-oxidation sample is also prepared for comparison.

Although the conventional gate re-oxidation makes oxide layer at the sides of gate electrode as shown Fig.1 (a), the modified gate re-oxidation method doesn't oxidize the sides as shown in Fig.1 (b). This is a very useful feature if tungsten poly-metal gate is applied to transistors in eDRAM. The conventional type gate re-oxidation process uses the selective oxidation method with $H_2O/H_2$ atmosphere in case of poly-metal gate [4]. The conventional type gate re-oxidation forms, however, oxide layer into the interface between tungsten and poly-Si layers as well as gate bird's beak. As a result, interface resistance at tungsten / Poly-Si layers might become higher. There is not such a bad influence if the modified gate re-oxidation process is applied.

## 3.Results and Discussion

Figure 4 shows $V_G$-$I_D$ characteristics. Figure (a) is the conventional gate re-oxidation sample and (b) is the modified one. Each figure compares two samples, $W_G$=5.0 and 0.3μm. In the conventional sample, the difference of $I_D$ at $V_G$=2.0V ($I_{ON}$) between $W_G$=5.0 and 0.3μm is a little more than one order. The difference of $I_D$ at $V_G$=-3.0V (GIDL) is almost the same. On the other hand, we can observe a large reduction of GIDL in the modified sample, about 2.5 orders, although the difference of $I_{ON}$ between $W_G$=5.0 and 0.3μm is a little more than one order. As a result, GIDL characteristics of the modified sample are superior to those of the conventional one at $W_G$=0.3μm. $I_{ON}$ ($V_G$=$V_D$=2.0V) and GIDL ($V_G$=$V_D$=-3.0V) are measured at various $W_G$'s, and their dependence on $W_G$ is plotted in Fig.5. $I_{ON}$ decreases in proportion to reduction of $W_G$ in both re-oxidation samples. GIDL of the conventional sample has the same property. On the contrary, GIDL of the modified samples decreases more rapidly than that of the conventional sample in the range of gate length ($L_G$)<0.3μm. This result suggests that amount of gate bird's beak by the modified process increases with decreasing of $W_G$, although the gate bird's beak by the conventional process doesn't depend on $W_G$. The schematic images of gate bird's beak are shown in fig.5. It can be said that it becomes easier for oxidant species to forms the gate bird's beak beyond the $Si_3N_4$ sidewall spacer in narrow $W_G$ transistor. This is because the oxidant species can reach the gate edges through trench isolation oxide on both sides. Consequently, it is possible to self-adjusts amount of gate bird's beak according to the $W_G$ value of each transistor. The modified gate re-oxidation process forms enough gate bird's beak for DRAM memory cell transistors (narrow $W_G$), and has little influence for random logic transistors (relatively wide $W_G$) which require thin $T_{OX}$.

Figure 6 shows the $I_D$ degradation by hot carrier (HC) injection. The modified sample has much better HC reliability than the conventional one. Because the modified sample has no oxide layer at gate sides and its gate / drain overlap length is larger, HC injection position is different from that of conventional one. That might be the cause of large improvement of HC immunity.

Figure 7 shows the dependence of GIDL and HC degradation on FO time in the modified gate oxidation process. As the FO time becomes longer, GIDL deceases, and HC reliability degrades a little. The degradation of HC immunity is probably caused by increase of mechanical stress. Figure 8 shows the stress simulation. The increase of FO time brings intensive stress especially near the drain edge, which degrades the HC immunity [5].

Figure 9 shows the result of dielectric reliability of gate oxide. It is confirmed that there is almost no difference between the modified one and conventional one.

## 4.Conclusion

The modified gate re-oxidation method, that is, the controlled furnace oxidation after the formation of $Si_3N_4$ sidewall spacer, forms gate bird's beak effectively for narrow gate width transistors. This method forms enough gate bird's beak selectively for DRAM cell transistors and suppresses their GIDL with no bad influence on high-speed logic transistors. HC reliability is also improved by this modified gate re-oxidation. Consequently, this new process realizes the ideal eDRAM.

**References**

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[2] K. Saino, et al., IEDM Tech. Digest, pp. 837-840, 2000
[3] K. Nojiri, et al., Ext. Abst. of 1985 SSDM, pp. 337-340, 1985
[4] I.-G. Kim, et al., IEDM Tech. Digest, pp. 615-618, 2001
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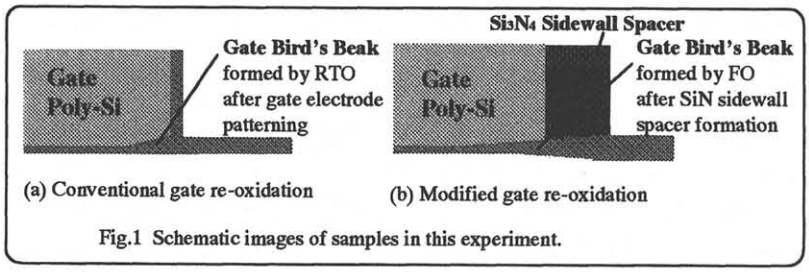



Fig.1 Schematic images of samples in this experiment.

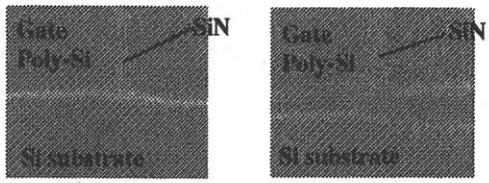



Fig.2 SEM images of gate edge before and after the modified gate re-oxidation process.

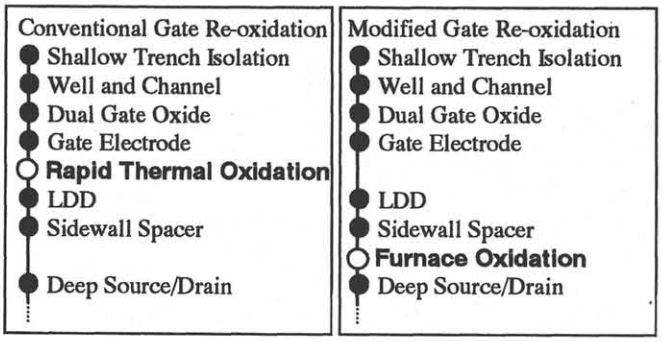



Fig.3 Process flow of conventional and modified gate re-oxidation method.

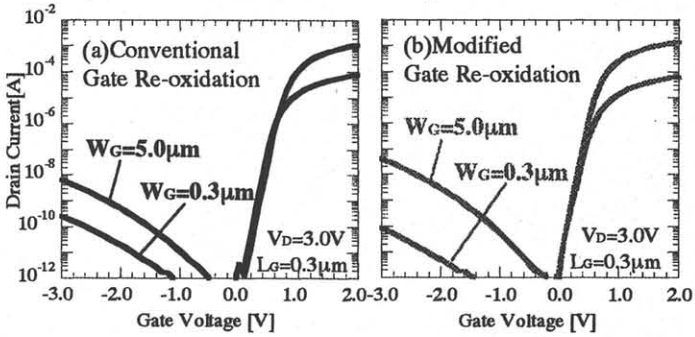



Fig.4 Comparison of VG-ID characteristics between conventional and modified gate re-oxidation samples. The modified gate re-oxidation sample improved GIDL current at narrow gate width MOSFET like memory cell transistor in the DRAM region.

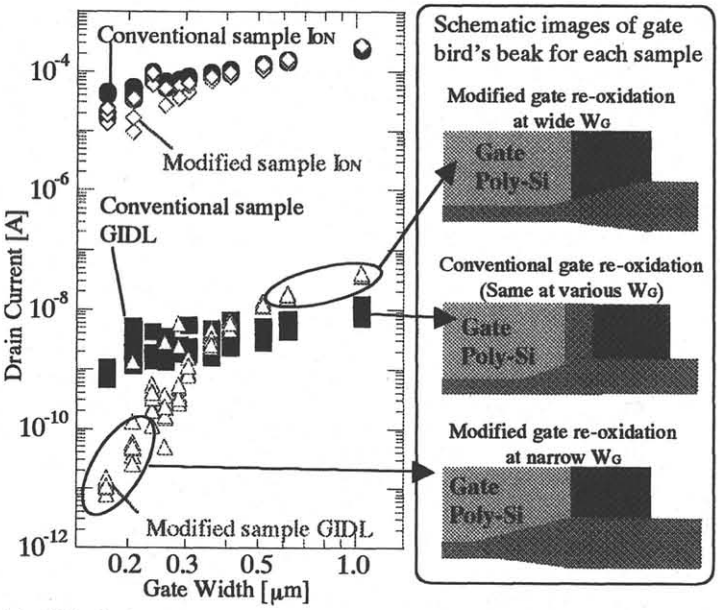



Fig.5 The Left graph shows gate width dependence of drain curre nts. The value of ION proportionately decreases by reduction of gate width in both con ventional and modified gate re-oxidation samples. On the other hand, the value of GIDL current rapidly decreases at small gate width region only in modified ga te re-oxidation sample. This suggests that the length of gate bird's beak changes in modified gate re-oxidation sample as shown in right schematic images.

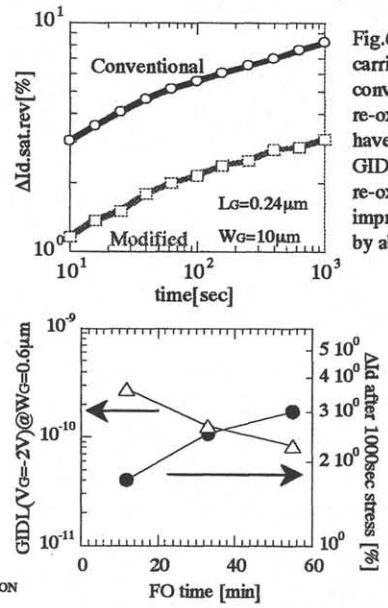
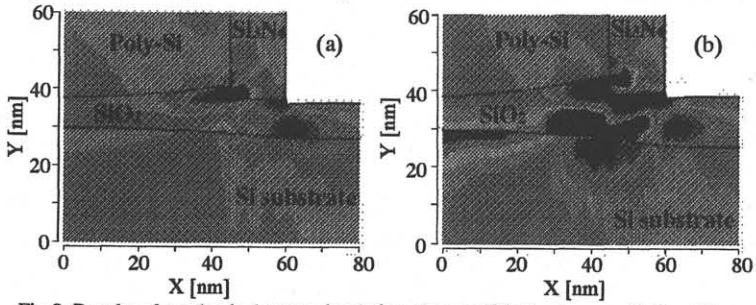



Fig.6 Comparison of hot carrier degradation between conventional and modified re-oxidation samples which have almost same ION and GIDL value. Modified gate re-oxidation sample improves degradation time by about 2 order.




Fig.7 The influence of gate re-oxidation time on GIDL current and hot carrier degradation. Although a large gate bird's beak reduces GIDL, it decreases hot carrier immunity.



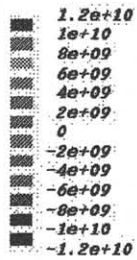




Fig.8 Results of mechanical stress simulation after modified ga te re-oxidation. The FO time of (b) is two times longer than that of (a). In fig.(b), stress value at gate edge is much larger than that of (b), which brings bat effects on hot carrier reliability.

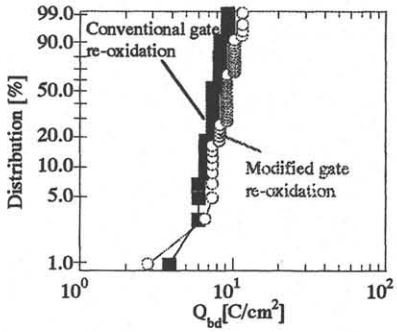



Fig.9 The result of dielectric reliability of gate insulator.