Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 690-691

A-7-2

Improvement of Disturbance/Pause Retention Time by Reducing Edge Channel Effect of Cell in Gigabit Density DRAMs and beyond

Il-Gweon Kim, Nam-Sung Kim, Young-Woo Kwon, Se-Kyung Choi, Jae-Soon Kwon, Young-Il Chun, Hee-Sik Yang, Jooseog-Park

Memory R&D Division, Hynix Semiconductor Co.,Ltd
1 Hyangjeong-dong Heungduk-gu Cheongju Chungbuk 361-480 Korea, e-mail: kigy@hynix.com

Introduction

As DRAM is scaled down into gigabit density, robust performance of disturbance characteristics as well as pause characteristics in retention time has been strongly demanded due to the requirement for low voltage operation and high reliability. However, if combined with anomalous VT(threshold voltage) lowering due to edge channel effect, shrinkage of DRAM cell is limited because of uncertainty in suppressing off-state leakage.[1][2] Bits of DRAM in a low cell VT state experience disturbing electric field when neighboring bits are operating, resulting in severely decreasing disturbance retention time. Thus, special care for edge channel effect in high density DRAM ce11 design should inevitably be taken. Edge channel effect, attributed to the STI(shallow trench isolation) geometry, has been significantly improved through improvement of STI corner rounding.[3] However, as SAC(self align contact) formation using CMP(chemical mechanical polishing) process in high density DRAMs has been preferred to etch back because of superior planarity and process stability, residual component migration path has become vulnerable to edge transistor effect. Also, path layers itself affect cell edge channel effect, depending on outguessing condition. Nevertheless, ILD layer related edge transistor effect has not been explained completely. Recent works report that STI-edge channel effect for periphery transistor is closely related to migration of residual chemistry components and moisture introduced by ILD (interlayer dielectric) layers into STI interface.[4] Since intriguing combination of various causes has become more and more complicated to identify edge channel effect of cell, effective cell structure, regardless of ILD layers process variation, to maintain the robust cell VT has been strongly demanded. Thus, cell design, based on blocking migration path, intensively was investigated. Furthermore, we proved that DRAM employing cell structure without edge channel effect enables to dramatically improve disturbance retention time, while still keeping superior pause retention time.

Cell scheme without abnormal edge channel effect

If ILD layers containing residual chemistry components and moisture, such as TEOS(tetraethyl orthosilicate)-based BPSG (boro phospho silicate grass) and SiH_4-based HDP(high density plasma) oxide, are capped with SiN as etch stopper material during capacitor formation, outgassing into air is completely blocked and diffusion into STI-edge region is occurred through the migration path exposed during CMP process. Upon CMP processing for SAC formation, STI-edge interface is connected to ILD layers by way of sidewall(SW) spacer LP-TEOS(Path2) and BPSG-barrier LP-TEOS(Path1).(Fig.1,2) Thus, cell scheme without abnormal edge channel effect is composed of only SW spacer SiN and only BPSG-barrier SiN to effectively block migration path with SiN. Prior to SW formation, gate re-oxidation more than 55 Å should surely be required not to be influenced by SiN layer induced stress. It has been reported that the origin of the degradation is attributed to the oxide-enhanced diffusion of boron by oxygen component contained in moisture [4]. A recent work shows that positive charges could be formed in the oxide by interacting with H_2 at a temperature over 500℃.[5] Judging from previous works, excessively moisture-contained BPSG without fully outgassing into air and excessively H_2-contained HDPoxide are considered to be major cause. Also, if path layers, composed of LP-TEOS, are not fully outgased, it may itself affect short channel effect. If the abnormal edge channel effect is removed, channel acceptor concentration can be reduced to a certain extent to keep cell VT beyond critical value by virtue of the removal of anomalous STI-edge channel effect. In addition, this enables to optimize disturbance retention time without the trade-off of pause retention time.

Experimental

0.15um-rule 128M DDR(Double Data Rate) DRAM, being quite stable in terms of technology maturity was used in this experiment. Technology is summarized in Table.1 In ILD process, reflowing in the ambient of steam after TEOS-based BPSG(ILD1) deposition was performed and CMP was followed for SAC formation. Then, the formation of the bitline(BL) of DRAM cell was performed and the second SiH_4-based HDP oxide(ILD2) was deposited. In order to verify edge effect dependence of cell transistor on migration path, several experiments with different cell structures were performed as shown in Table.2. In addition, cell scheme without abnormal edge channel effect is compared to the conventional scheme in total device performance point of view, including retention time, injected hot-carrier degradation and cell leakage. Furthermore, variation of retention time caused by dynamic circuit degradation under wafer burn-in stress was evaluated.

Results and Discussion

As a result of TDS(Thermal Disorption Spectroscope) analysis, ILD layers are mainly composed of H_2O[moisture] with trace residual compounds such as CO/CO_2/ C_xH_y and H_2.(Fig.3) TEM images for conventional and cell without abnormal edge channel effect are shown in Fig.4. Edge channel phenomena in I-V curve of cell transistor with long width [W/L=12/0.15] appears to be distinguishable while cell transistor with short width [W/L=0.18/0.15] is totally affected by edge channel effect, resulting in anomalous parallel VT shift in I-V curve.(Fig.5,6) In order to clearly verify edge channel phenomena in I-V curve, cell transistors with different dimension are chacterized by H-parameter method.(Fig.7)[6]. Anomalous VT lowering is dramatically improved by cutting off migration path. Failure during BL disturbing stress is a strong function of cell VT and Vp-t(punch-through voltage) as shown in Fig.8. Cell leakage for proposesd cell scheme(Type-III) was characterized using 4K array test pattern. Fig.9 shows that there is no degradation of cell junction leakage, compared to conventional structure. Decrease from 1.3E13/ cm^2 to 1.1E13/cm^2 makes it possible to improve tail component of pause retention time further(20%) by synergy effect combined with less junction electric field(Fig.10). Upon on/off read toggling of 80ms per WL1(wordline) and WLn-1, all cell transistor connected with all BL in enable state, were influenced by the disturbance stress and stored data in the low VT cell were lost by enhancing off-state and punch-through leakage.(Fig.11) When the channel dose is optimized to 1.1E13/ cm^2, the number of failure bit stemmed from BL disturbance stress was dramatically reduced, resulting in improving disturbance retention value @1E-4% fail bit by 50%.(Fig.12) In addition, variation of retention time from dynamic cell stress using the wafer burn-in mode, consisting of full BL Vss/Vcore toggling stress in all WL enable state of fixed Vpp=5.2V, was not noticeable.(Fig.13)

Conclusion

We have investigated the cell structure for suppressing anomalous VT lowering due to edge channel effect to improve data retention time in gigabit density DRAM. Our work verifies that insufficient outguessed ILD layers affects edge channel effect, strongly depending on the presence of migration path toward edge channel region. Thus, effective cell structure, regardless of ILD layers process variation, to maintain the robust performance of cell VT is suggested, which is designed on the basis of blocking migration path. Additionally, cell structure without abnormal edge channel effect makes it possible to improve both disturbance retention time @1E-4% by 50% and pause retention @1E-4% by 20% for 128M DDR DRAM with 0.15um-design rule and COB(capacitor over bitline). Proposed cell scheme shows no degradation in total device performance point of view including cell leakage. Furthermore, retention time degradation stemmed from the dynamic cell stress using wafer burn-in mode is not remarkable.

References

[1]. I.G Kim, *et al.*, IEEE , VLSI Tech.Dig. 2000, p86.
[2]. K.N Kim, *et al.*, IEEE , VLSI Tech.Dig. 2001, p7.
[3]. M.Nandakumar, *et al.*, IEEE , IEDM Tech.Dig. 1998, p133.
[4]. S.K Park , *et al.*, IEEE , IRPS Tech.Dig. 2000, p164..
[5]. V.V.Afanas'ev,*et al.*, Appl.Phys.,Lett., Vol.72, p.79,1998
[6]. H.Brut,*et al.*,IEEE *Int.Conf. on Microelect. Test Struct.*,Vol 12, p188, March 1999

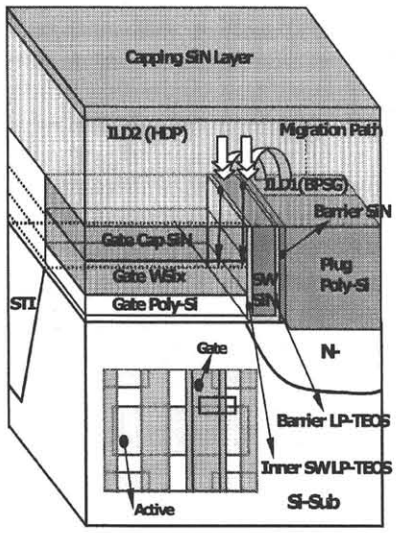


Fig.1 Schematic concept of anomalous cell VT lowering due to edge channel effect.

Table1 Technology summary

Memory cell structure	Capacitor Over Bit Line
Design rule	0.15um
Isolation	Shallow Trench Isolation
Gate oxide thickness	6.5nm
Gate stack layer	Wsi/poly/SiO2
Cell Storage Node Cont	SAC (Self-Aligned Contact)
Capacitor dielectric	ON dielectric

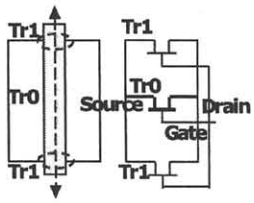


Fig.2 Equivalent circuit for edge channel effect of cell transistor.

Table 2. Split condition

Split condition	Gate inner SW spacer layer	BPSG-barrier layer	Gate re-oxidation	Channel implant dose
Normal	LP-TEOS(90 Å)	LP_TEOS(60 Å)/ SiN(150 Å)	32 Å	1.3E13/cm2
Type-I	LP-TEOS(90 Å)	SiN(150 Å)	32 Å	1.3E13/cm2
Type-II	skip	SiN(150 Å)	32 Å	1.3E13/cm2
Type-III	skip	SiN(150 Å)	55 Å	1.1E13/cm2

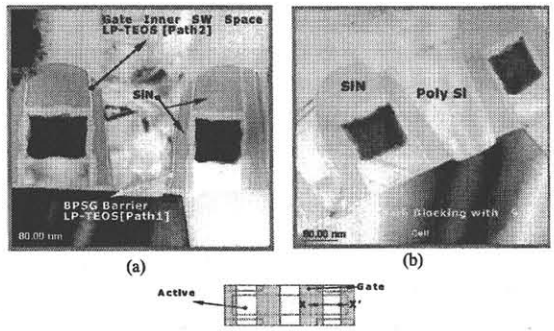
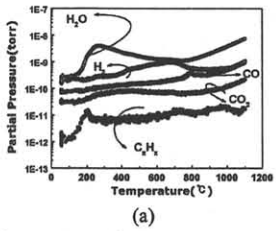


Fig4. TEM images for migration path of moisture and chemistry component contained in ILD. ILD layers are connected to STI edge, through SW spacerr LP-TEOS(Path2) and BPSG-barrier LP-TEOS(Path2)
(a) conventional structure (b) cell structure without edge channel effect(Type-II)



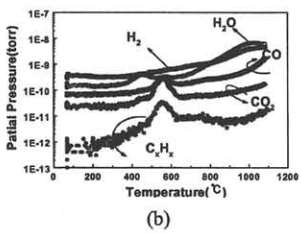
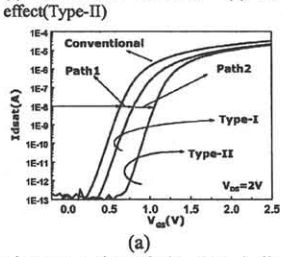


Fig.3. TDS analysis for TEOS-based BPSG layer[ILD1](a) and SiH4- based HDP(b).



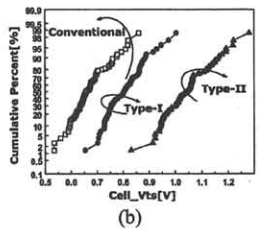
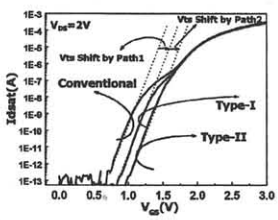
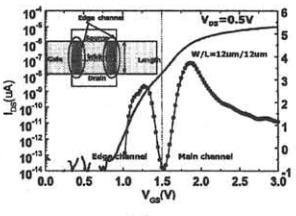
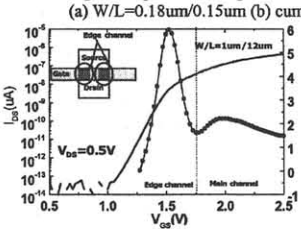


Fig.5 Comparison of edge channel effect for three different cell schemes.
(a) W/L=0.18um/0.15um (b) cumulative plot.







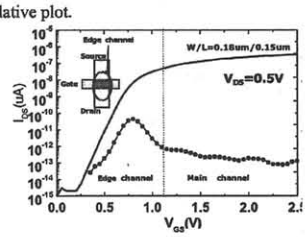
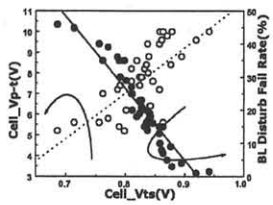
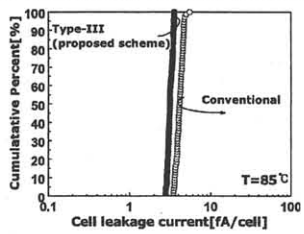
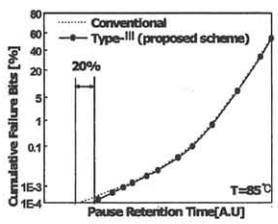


Fig.6 Comparison of edge channel effect for three different cell schemes, based on.W/L=12um/0.15um.

Fig.7. Edge channel phenomena in I-V curve of cell transistor with long width appears to be distinguishable while cell transistor with short width is totally affected by edge channel effect, resulting in anomalous parallel VT shift in I-V curve. Edge channel effect is chacterized by H-parameter method, based on linear region: $H(V_G) = d(-\log(Gm/I_D))/dV_G$ [6].
W/L=12um/12um (a) 1um/12um (b) 0.18um/0.15um (c)







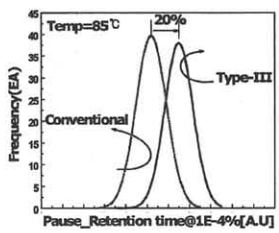
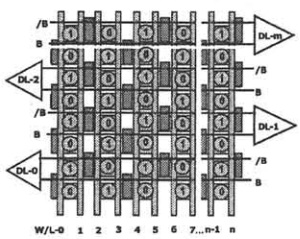
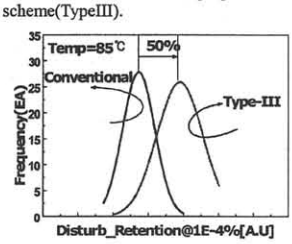


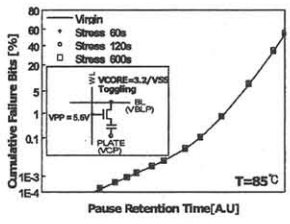
Fig.8 BL disturbance fail rate is a strong function of cell VT and Vp-t.

Fig.9 Comparison of cell leakage between conventional and proposed cell scheme(TypeIII).

Fig.10 Comparison of pause retention distribution between conventional and proposed cell scheme(TypeIII)







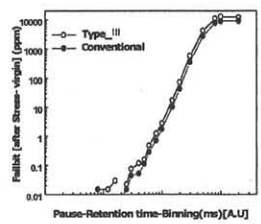


Fig.11 Schematic concept of BL disturbing stress.

Fig.12 Comparison of disturbance retention distribution between conventional and proposed cell scheme(Type-III)

Fig.13 Variation of retention time from dynamic cell stress using the wafer burn-in mode. (a) as a function of stress time. (b) Based on 600sec-stress, microscopic failbit variation for convetional and proposed cell scheme(Type-III).