Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 692-693

A-7-3

Impact of Burn-In Stress on Reliability of High Density DRAMs

Il-Gweon Kim, Jun-Hyun Chun, Nam-Sung Kim, Young-Woo Kwon, Se-Kyoung Choi, Joo-Seog Park

Memory R&D Division, Hynix Semiconductor Inc.
1 Hyangjeong-dong Heungduk-gu Cheongju Chungbuk 361-725 Korea, e-mail:kigy@hynix.com

Introduction

In order to maintain a satisfactory reliability level of DRAM, effective wafer burn-in (WBI), prior to die sorting, has been reported. Upon WBI testing, known failure bit addresses are replaced by spare row and column, resulting in reducing package burn-in (PBI) time and minimizing the number of abandoned chips. This enables to improve totally yield, while keeping low test and assembly cost. Also, PBI has become a critical ingredient to screen reliability failure in high density DRAMs. Recently, PBI test incorporating the effective WBI is known as the attractive screen method. Nevertheless, burn-in condition is strictly limited because of a potentially adverse effect, such as the degradation of retention time stemmed from dynamic operation stress.[1] In the stage of technology qualification, both WBI and PBI condition is strictly selected to satisfy early failure rate (EFR). Thus, a total of chip is exposed to severe burn-in (BI) stress and suffers from potentially adverse effect. Static BI stress condition for screening gate dielectric/storage capacitor and various SAC(self aligned contact) BV(breakdown voltage) is carefully considered not to worn out with regard to dielectric lifetime. However, dynamic operation stress introduced during the PBI is not enough explained. Thus, in this paper, equivalent stress in wafer level, which corresponds to PBI stress, is realized and characterized from the viewpoint of retention time degradation. Furthermore, its relationship of wafer level test with package level test is investigated in terms of dynamic operation stress, for the first time. On the basis of WBI test, both dynamic and static stress are analyzed and relevant condition of BI is intensively studied.

Experimental

0.15um-ruled 256M DDR(double date rate) DRAM with STI was used in this experiment. Technologies are summarized in Table 1. Circuit is implemented to concurrently realize both static stress and dynamic stress in wafer level. Equivalent stress, corresponding to PBI stress, is applied all together to full mat of DRAM. BI dynamic operation stress is characterized from the viewpoint of retention time degradation. In order to verify the impact of dynamic operation stress on reliability of DRAM product, two different devices (Table 2), with regards to interface quality of gate overlapped region, are intentionally fabricated and compared.

Circuit Implementation

Circuit implementation is conceptually shown in Fig.2. WBB is used as a pad to enable WBI mode. Various commands in WBI mode are decoded using the rest of pads. A BL(bitline) potential is controlled by VBLP(bitline precharge voltage) If every WL(wordline) are active state and test command signals (TVBLPSTB, TVBPL, TVBLPH) are given, switching stress is applied to BL in form of VSS-VCORE(3.2V) toggling. WL voltage level(VPP=5.6V), higher than normal VPP, is selected to apply static stress. Equivalent stress time in wafer level, corresponding to PBI stress, is roughly estimated, by dividing total PBI time by the number of total WL.

Results and Discussion

Comparison of PBI failure as a funtion period is shown in Fig.1 One is put into WBI prior to die sorting and the other is not. In case of PBI test incorporating WBI, failure bits are saturated as a function of PBI stress time. Circuit implementation is shown in Fig.2 Rentention variation after WBI stress is chacterized with initial curve included for comparison.(Fig.3). We verified that dynamic operation stress was closely correlated with rention time degradation in microscopic failbit range, strongly depending on stress time. Stress, more than 120sec, causes drastically the increase of failure bit, which is responsible for dynamic operaton induced HC (hot carrier) degradation.[2] This indicates that BI operation time should be carefully limited not to exeed 120s per cell at 125 ℃. In order to clarify the impact of dynamic operation stress on reliability, two devices having differnet cell structure with regards to interface quality of gate overlapped region, were intentionally fabricated and compared. Type-I device deliberately deteriorates interface quality by enhancing SiN stress. These differences are confirmed by electrical characterization, such as GIDL (gate induced drain leakage) and HC degradation of cell. At the bias of V_{GS}=0, V_{DS}=5V, GIDL for Type-II device shows a superior result to that for Type-I as shown in Fig.4 (a). Cumulative characteristics of VT shift due to the localization of trapped carriers after HC stress in cell transistor (V_{DS}=3.2V,V_{GS}=1.6V, Time=60s) is observed in Fig.4 (b). [3] The maximum surstrate current condition at V_{DS}=3.2V and V_{GS}=1.7V was chosen for severely accelerating HC stress. Based on VPP=5.6V,VCORE=3.2/VSS and stress time=120s, retention time for virgin device and WBI stressed device is characterized, respectively (Fig.5,6). Type-I device showes severe deterioration of retention time, compared to Type-II.(Fig.7) This is well consistent with GIDL and HC characteristics. Package failure rate confirms that dynamic operation stress affects retention deterioration (Fig.8). This is a good agreement with WBI-stressed results.

Conclusion

Circuit to concurrently realize both static and dynamic stress in WBI mode is successfully implemented, for the first time. We verify that retention time degradation occurred during PBI test is attributed to dynamic operation-induced HC stress. Impact of dynamic operation stress on reliability of DRAM is proved through intentionally fabricated devices. As a result, retention time degradation after WBI stress is strongly dependent on interface quality around gate overlapped region. Also, variation of electrical characteristics in wafer level is good agreement with that in package level chracteristics. BI operation time at 125 ℃ should be carefully limited not to exeed a crtical value. Otherwise, retention time is deteriorated by the BI stress, resulting in decreasing totally product yield.

References

[1]. Yoonjong Huh,et al., IEDM Tech. Dig., p33. 1995
[2]. M. Brox,et al., IEEE/IRPS,.p.133,1991
[3]. Nam-Sung Kim et. al., SSDM,.p.28,2001

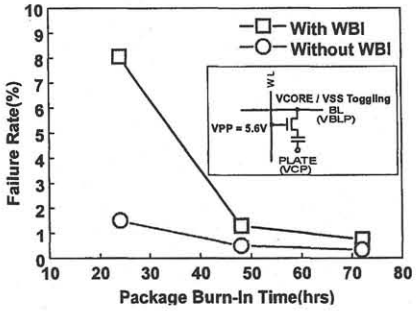
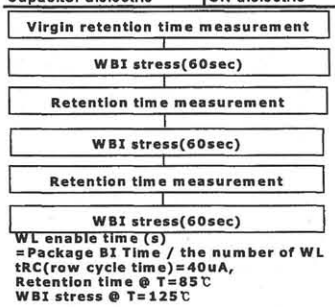


Fig.1 Comparison of PBI failure rate as a funtion of time: One is put into WBI prior to die sorting and the other is not.

Table1 Technology summary

Memory cell structure	Capacitor Over Bit Line
Design rule	0.15um
Isolation	Shallow Trench Isolation
Gate oxide thickness	6.5nm
Gate stack layer	WSi/poly/SiO_2
Cell Storage Node Contac	SAC (Self-Aligned Contact)
Capacitor dielectric	ON dielectric



(a)

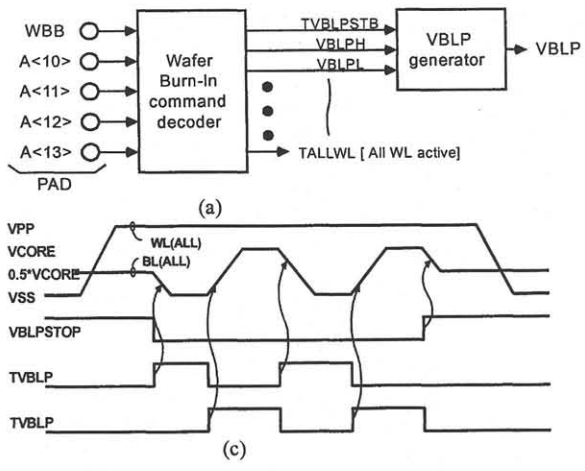
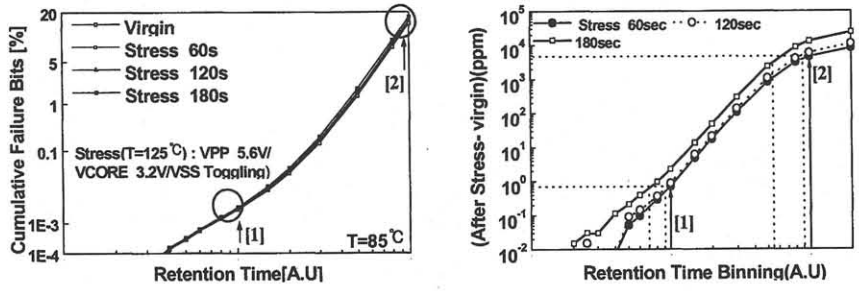
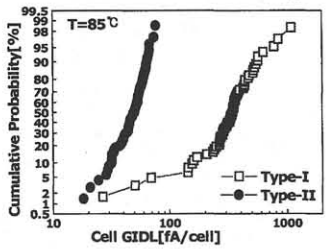


Fig.2 Circuit implementation (a) WBI command decorder (b) BL potential is controlled by VBLP(bitline precharge voltage). (c) BL toggling pattern (d) Under WL enable state, VBLP is toggled between VCORE and VSS.

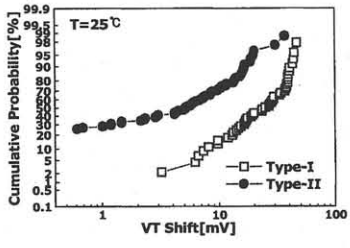


(a) (b) (c)

Fig.3 Rentention variation after WBI stress is chacterized with initial curve included for comparison. (a)WBI stress sequence (b) Macroscopic variation of failure bits is not remarkable. (c) Microscopic variation of failure bit as a function of stress time. Stress more than 120sec causes drastically the increase of failure bit, which is responsible for dynamic operaton induced HC degradation.[2]



(a)



(b)

Table. 2

Split condition	Cell gate SW spacer layer	Cell gate re-oxidation
Type-I	LP-SiN(500Å)	32Å
Type-II	LP-TEOS(90Å)/ LP-SiN(450Å)	55Å

Fig.4 Impact of dynamic operation stress on reliability of DRAM is proved through intentionally fabricated devices.(Table2) Type-I device deliberately deteriorates interface quality by enhancing SiN stress, compared to Type-II. (a)Comparison of GIDL current at the bias of V_{GS}=0, V_{DS}=5V. (b) Cumulative characteristics of VT shift due to the localization of trapped carriers after HC stressing in cell transistor (V_{DS}=3.2V,V_{GS}=1.6V, Time=60s)

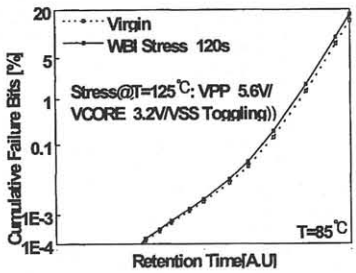


Fig.5 Retention time characteristics for virgin device and WBI stressed device (stress time=120s) is shown for Type-I devices.

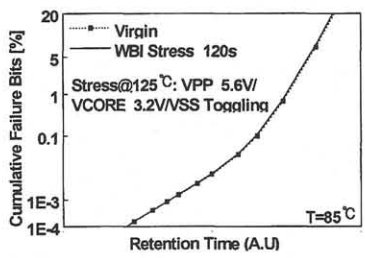


Fig.6 Retention time characteristics for virgin device and WBI stressed device (stress time=120s) is shown for Type-II device.

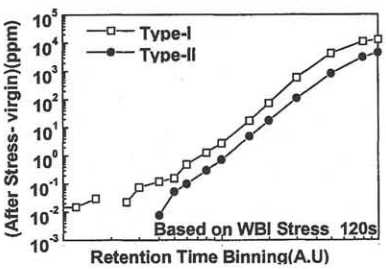


Fig.7 Microscopic variation of failure bit after WBI stress 120sec is compared for two different devices. Type-I device shows severe deterioration of retention time, compared to Type-II.

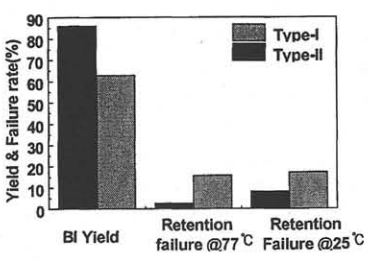


Fig.8 Comparison of PBI yield and retention failure for two different devices. This is a good agreement with WBI-stressed results.