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# Field-Shield Trench Isolation with Self-Aligned Field Oxide

Akihiro Takase*[1], Toshirou Kidera*[2], and Hideo Sunami

Hiroshima University, Research Center for Nanodevices and Systems
1-4-2 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8527, Japan
Phone: +81-824-24-6269, Fax: +81-824-22-7185, e-mail: sunami@sxsys.hiroshima-u.ac.jp

## 1. Introduction

In response to the requirement to denser packing of LSI's, shallow trench isolation has been developed along with active device shrinkage. The trench isolation has already been applied to products however, its $SiO_2$ filling requires very critical control in processing to avoid anomalous recess and void causing well-known "hump current" in $I_d$-$V_g$ characteristics [1]. Besides, a big difference in thermal expansion coefficients of Si and $SiO_2$, the $SiO_2$ filling also needs critical control to avoid crystal defects [2] which may cause fatal leakage current.

In this presentation, a novel fabrication technique is proposed providing polysilicon-filling trench isolation with "humpless" $I_d$-$V_g$, potential low-stress, and low-parasitic capacitance. Although the structure itself was already proposed [3], this study introduces a novel self-aligned formation of isolation oxide. This structure provides adequate isolation characteristics with low electric-field penetration [4] and low punchthrough current due to the polysilicon field shield.

## 2. Device Fabrication

Trench and LOCOS structures are fabricated on a same wafer. A fundamental process sequence for the trench is shown in Fig. 1. After trench etching, the trench surface is oxidized to be 10 nm in thickness and filled with polysilicon. Then, the polysilicon is heavily doped with phosphorus. The thickness of $Si_3N_4$ sidewall spacer and the residual thickness of the polysilicon shown in Fig. 1 (5) should be controlled precisely to achieve desirable structures. An obtained isolation cross-section is shown in Fig. 2.

As heavily doped impurities significantly enhance wet oxidation rate [5], this impurity-enhanced oxidation (IEO) is utilized to obtain relatively thicker oxide on the isolation region compared to thinner oxide on active region. Figure 3 shows a part of experimental results of IEO obtained in this study. The enhancement ratio increases with the increase in impurity concentration and the decrease in oxidation temperature [5]. TEM micrographs of the obtained structure are shown in Fig. 4.

## 3. Device Characteristics

### *1) Transistor characteristics*

The $I_d$-$V_g$ subthreshold characteristics for n-MOS transistors, as shown in Fig. 5, give rise to no "hump current" suggesting that trench edges are covered with thick oxide. Only in case of 0.1-μm channel width slight hump can be observed.

Gate leakage current characteristics are measured for striped patterns as shown in Fig. 6. The fact that the circumference length of gate region has no adverse effect may suggest that trench edges are fully covered with thick oxide avoiding electric-field concentration on the edges.

### *2) Isolation performance*

Leakage currents between two adjacent $n^+$-junctions across the trench and LOCOS are shown in Fig. 7. Since the filled polysilicon works as a field shield with $V_{sub}$ potential, the trench is far superior to LOCOS.

Capacitances of striped junctions are measured and shown in Fig. 8 for both structures. It is obvious that observed capacitances of the trench are smaller than those of LOCOS. It is speculated that elevated channel stopper by about 0.6 μm below the LOCOS oxide may increase fringe capacitance, $C_F$ leading to total capacitance increase, while the junction-to-shield overlap capacitance is relatively smaller than the fringe capacitance.

### *3) Thermal budget robustness*

It is widely known that generation of detrimental dilocation along field oxide edges is very susceptible to stress arisen from big difference of thermal expansion coefficients of Si and filled $SiO_2$. Thus, thermal budget together with structure itself should be carefully designed. An $SiO_2$ filling trench isolation is not realized yet in this study however, it is observed that LOCOS with 200-nm thick $SiO_2$ and the polysilicon field shield with 100-nm thick $SiO_2$ are almost equivalent in terms of wafer warpage in a preliminary experiment. Further investigation should be required.

## 4. Conclusion

A novel fabrication technique for sub-μm trench isolation is proposed featuring polysilicon field shield and thick isolation oxide formed with impurity-enhanced oxidation. Device performance is satisfactory in terms of hump current reduction, gate leakage current suppression, and reduced junction parasitic capacitance. In addition, less susceptibility to crystal defect generation can be expected due to low stress inherent to polysilicon filling.

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Present addresses : *[1] Toshiba Corp., Semiconductor Company, *[2] Fujitsu Ltd., Electronic Devices Group.

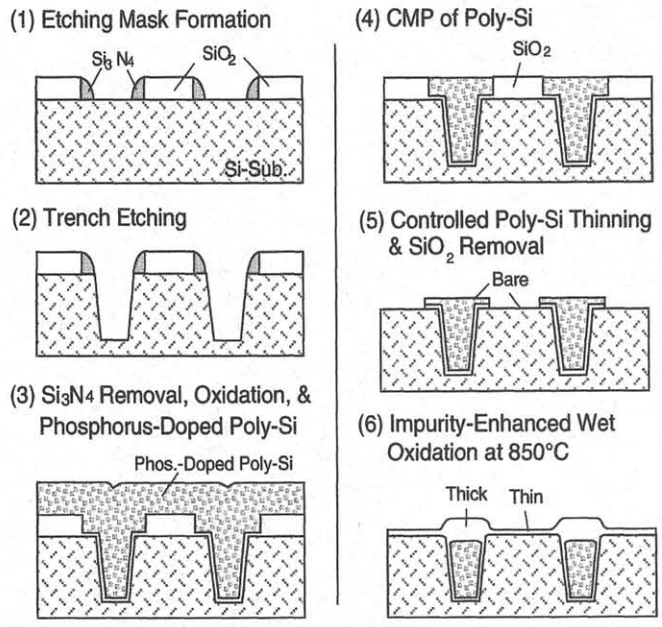



Fig. 1 A process sequence for proposed plolysilicon-shield trench isolation utilizing impurity-enhanced oxidation.

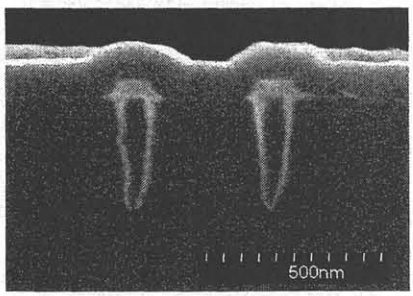



Fig. 2 SEM micrograph of obtained 0.1-μm wide polysilicon shield trench isolation of which shoulders are covered with thick oxide.

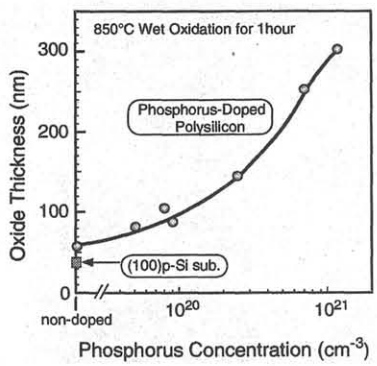



Fig. 3 Impurity Enhanced Oxidation (IEO) for 1 hour at 850°C in wet oxygen (40% $H_2O$).

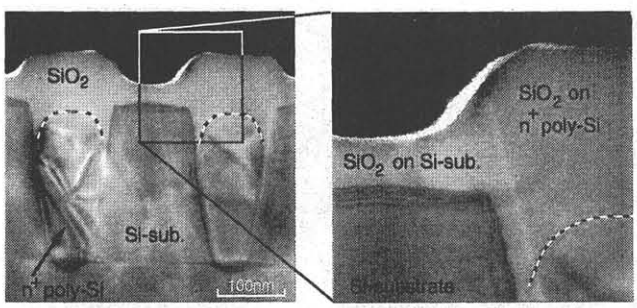
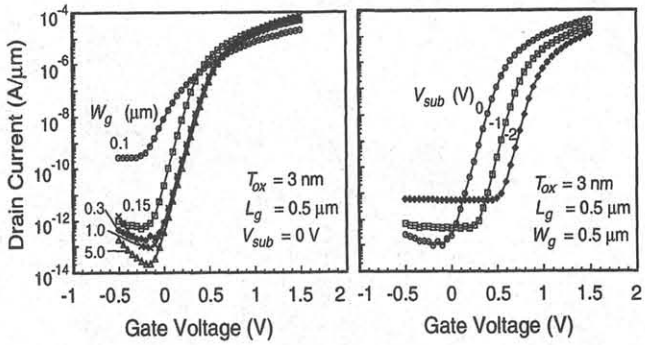



Fig. 4 TEM micrographs show conformal oxide formation along trench edges. Broken lines indicate oxidized polysilicon surfaces.




(a) Channel Width Dependence (b) Substrate Bias Dependence

Fig. 5 Dependences of channel width (a) and substrate bias (b) on $I_d$-$V_g$ characteristics of active transistors with the field-shield trench. A small "hump current" is only observed for 0.1-μm $Wg$.

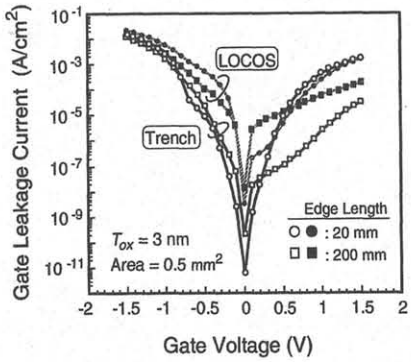



Fig. 6 Gate leakage currents of striped active regions for trench and conventional LOCOS isolation structures.

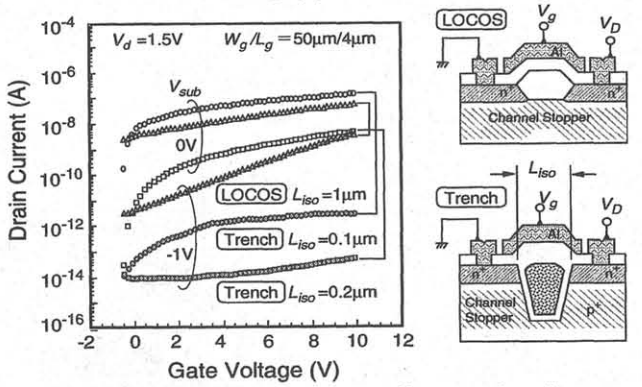



Fig. 7 Leakage currents between two adjacent n+-junctions across isolation regions.

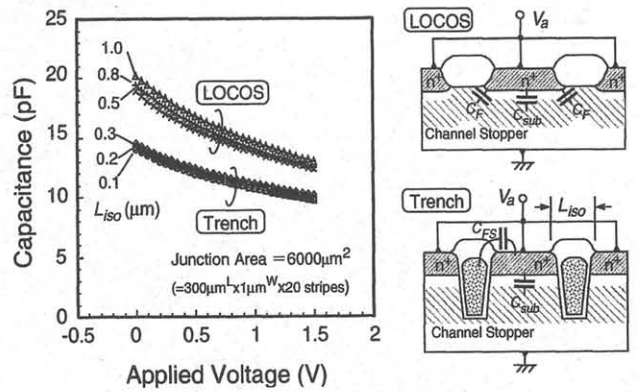



Fig. 8 Observed capacitances of multi-striped n+-junctions for the trench and LOCOS. Boron was implanted at 85 keV with a dose of $9x10^{12}$ $cm^{-2}$ after LOCOS formation and before trench etching.