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# Voltage Acceleration of Ultra-Thin Gate Oxide Degradation before and after Soft Breakdown

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## 1. Introduction

It has been reported that MOSFET devices remain functional even after the occurrence of soft breakdown (SBD) in thin gate oxide [1,2]. However, the current leakage through SBD spots increase total gate current in a LSI chip, resulting in excess power consumption [3]. As shown in Fig. 1(a), in the case of thick oxides stressed with high voltage, the oxide conductivity jumps abruptly (within ~ 10 $\mu$s [4]) just after SBD. However, this is not the case for ultra-thin oxides subjected to breakdown under low stress bias; after SBD the gate current, $I_g$, increases gradually [5] as illustrated in Fig. 1(b). This also leads to the gradual increase of the dissipation power in a chip. However, to the best of the authors' knowledge, there have been no reports on the analysis of the leakage current evolution after SBD.

The aim of this study is, therefore, to investigate the post-SBD degradation of ultra-thin gate oxides, particularly focusing on the acceleration characteristics of the gate leakage current under voltage stress.

## 2. Experimental

The devices used were MOS capacitors with $n^+$ poly-Si gate fabricated on p-Si substrate. The gate dielectrics were either pure $SiO_2$ or oxynitride with the thickness of 1.5 - 2.8 nm. Small capacitors (1×1, 5×5, or 20×20 $\mu m^2$) were used to minimize the effect of series resistance. The time evolution of gate current under constant voltage stress (CVS) was monitored before and after SBDs.

## 3. Results and Discussion

Figure 2 shows the measured $I_g$ *vs.* stress time as a parameter of stress gate voltage, which represents the gradual increase of the gate current, $I_g$. We used a stress interruption technique shown in Fig. 3 to extract the voltage acceleration rate of the post-SBD degradation from the experimental data measured under various stress conditions. The interruption technique significantly reduces the measurement time, especially, under low bias conditions, otherwise, one requires unrealistic long experiment time to induce SBD. We first apply high voltage stress to the samples until the occurrence of SBD and then we switch over to lower voltage stresses to the same samples after SBD. We confirmed through experiments that this high-to-low stress transition dose not affect the post-SBD results.

Figure 4 shows the time evolution of $I_g$ for post-SBD oxides stressed under various low voltages. The log $I_g$ *vs.* $\log(t - t_{SBD})$ characteristics are well fitted with a linear function [3], and their slopes, 0.2, is independent of the stress voltage. As illustrated in Fig. 5, the SBD duration time, $t_{post\text{-}SBD}$, is defined as a time when $I_g$ reaches a given value, that is, three times as much as the background leakage current in the present study. Figure 6 shows $t_{post\text{-}SBD}$ and $t_{SBD}$ as a function of $V_g$. Both $t_{post\text{-}SBD}$ and $t_{SBD}$ increase exponentially with decreasing $V_g$, and the voltage acceleration factors, i.e. the slopes on a log $t$-$V_g$ plot, are very similar between the two characteristic times of oxide degradation before and after SBDs. This indicates that a common origin involves in oxide degradation processes before and even after SBD. Moreover, if the measured $I_g$ shown in Fig.2 are shifted by the amount of their corresponding $t_{SBD}$, all the data are very close to a universal curve. This fact further supports that the common origin is involved in the degradation.

As illustrated in Fig. 7, the lifetime of a chip can be estimated from the measured $t_{SBD}$ because the lifetime, the sum of $t_{post\text{-}SBD}$ and $t_{SBD}$, is only a parallel upward shift of $t_{SBD}$ *vs.* $V_g$ characteristics due to their common origin.

## 4. Conclusions

We have investigated the gate voltage acceleration characteristics of the time degradation for the ultra-thin oxides after SBD in detail for the first time.

We found the following features:

- The log $I_g$ *vs.* $\log(t - t_{SBD})$ characteristics after SBD are well fitted with a linear function, and their slopes are independent of $V_g$.
- Two characteristic times for the oxide degradation before and after SBD exhibit similar dependence of $V_g$, implying the same type of degradation mechanism involved.

## Acknowledgement

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## References

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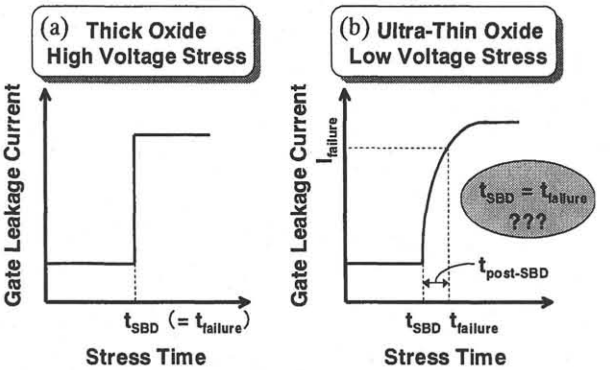


Fig. 1 Schematic illustration to compare the time evolution of gate current after SBD induced by (a) high and (b) low stress voltages.

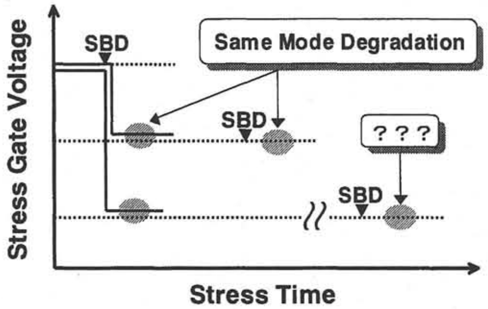


Fig. 3 Schematic drawing for the stress interruption technique (solid line) and the conventional CVS (dashed line). SBD is induced by using a high stress voltage, and then a low bias is applied to investigate the post-SBD degradation.

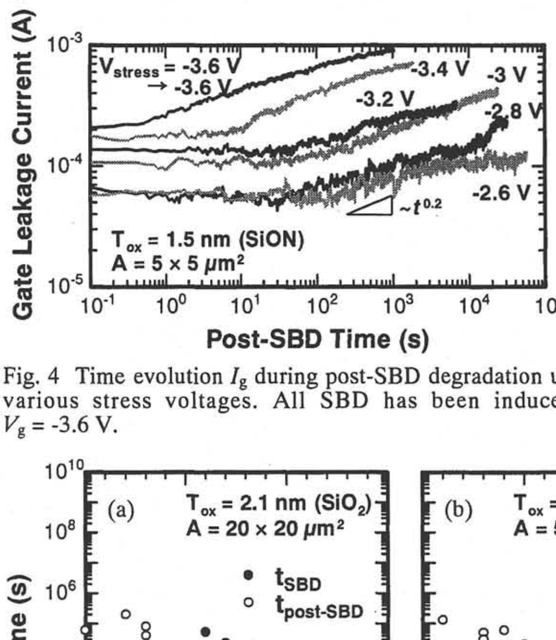


Fig. 4 Time evolution $I_g$ during post-SBD degradation under various stress voltages. All SBD has been induced at $V_g$ = -3.6 V.

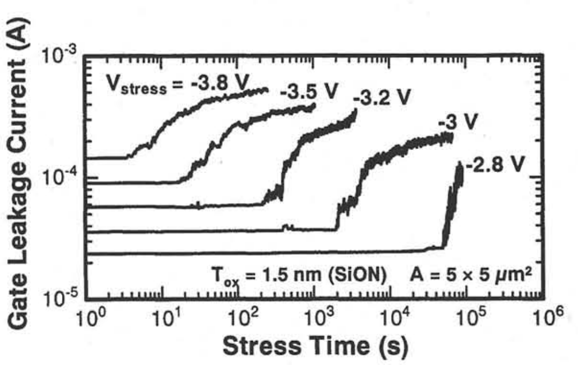


Fig. 2 Time evolution of gate current before and after SBD under various stress voltages. The degradation rate is slower for lower stress voltages.

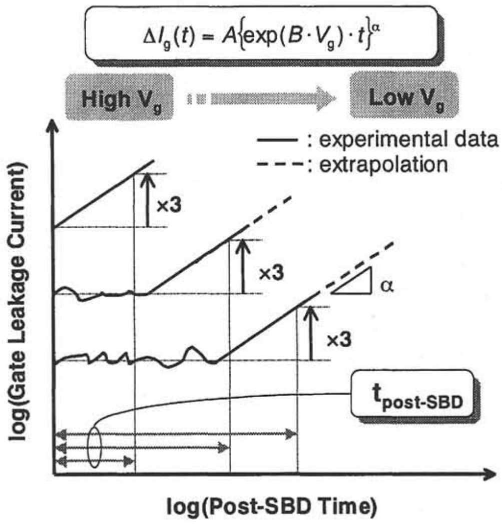


Fig.5 Schematic illustration to show the post-SBD degradation. $I$ versus $t$ characteristics are well expressed by a power law. $t_{post\text{-}SBD}$ is defined as a time for $I_g$ to increase by a given factor from its initial value.

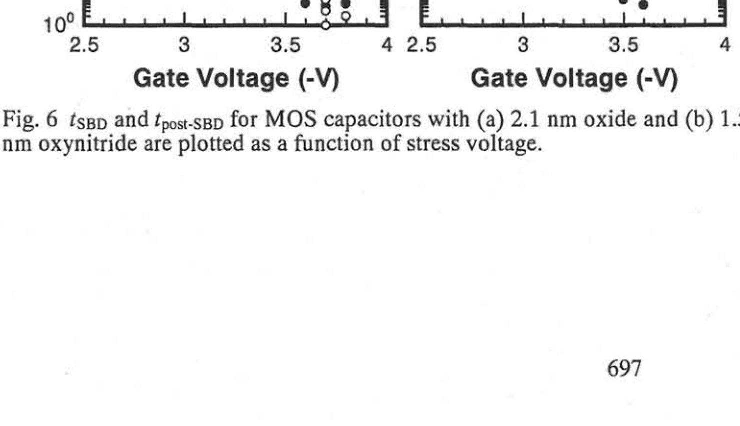


Fig. 6 $t_{SBD}$ and $t_{post\text{-}SBD}$ for MOS capacitors with (a) 2.1 nm oxide and (b) 1.5 nm oxynitride are plotted as a function of stress voltage.

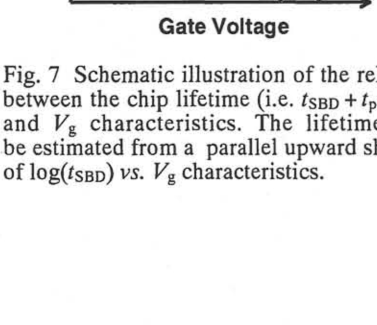


Fig. 7 Schematic illustration of the relation between the chip lifetime (i.e. $t_{SBD} + t_{post\text{-}SBD}$) and $V_g$ characteristics. The lifetime can be estimated from a parallel upward shift of log($t_{SBD}$) *vs.* $V_g$ characteristics.