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Oxide Soft Breakdown Effects on Drain Current Flicker Noise in Ultra-Thin Oxide CMOS Devices

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Abstract

Impact of oxide soft breakdown on drain current flicker noise in ultra-thin oxide nMOS and pMOS transistors is investigated. As compared to nMOSFETs, pMOSFETs exhibit significantly larger flicker noise degradation after soft breakdown. Our study reveals that the increased low-frequency noise in pMOSFETs is attributed to non-uniform threshold voltage distribution resulting from positive oxide charge creation in the soft breakdown spot.

Introduction

Flicker noise of drain current in CMOS transistors is an important parameter for the design of high performance RF and mixed mode circuits. Previous study has shown that flicker noise decreases as gate oxide thickness reduces [1]. However, it is known for years that thinner oxides exhibit anomalous wear-out phenomena, referred to as soft breakdown (SBD). It has been reported that SBD can degrade gate signal noise [2]. The SBD effects on drain current flicker noise, however, are rarely studied.

In this work, nMOS and pMOS transistors with 20Å gate oxide are studied. The gate length is 0.12μm and the gate width is 10μm and 1μm. The devices were stressed at constant voltage. The noise behavior of the devices during stress is characterized. The input referred noise power spectrum density (S_{vg}) is used as a monitor of drain current noise degradation, which is considered to be a fair index because of the normalization of the drain current.

Results and Discussion

Fig 1. shows stress current versus time in nMOS and pMOS transistors (W/L=1μm/0.12μm) at constant voltage stress. Both devices show gate current fluctuations when SBD occurs. The drain current flicker noise is measured in the linear operation region at four measurement times, $t=t_0$ (fresh), t_1 (pre-SBD), t_2 (post-SBD) and t_3 (hard breakdown), as illustrated in Fig. 1. Fig 2. shows the measured noise characteristics of the pMOSFET. The noise remains almost the same before SBD ($t=t_0$ and t_1) and suddenly increases after SBD ($t=t_2$ and t_3). In contrast, the drain current noise of the nMOSFET (Fig. 3) is about the same at all the measurement times. In addition to noise, we monitor the corresponding Vt shift (Fig. 4 and Fig. 5). As shown in Fig 4., the pMOSFET has a relatively small Vt shift from t_0 to t_1 and then exhibits a rapid increase in Vt after SBD ($t=t_2$). The Vt shift in the pMOSFET can be realized due to positive oxide charge creation by stress. However, it should be emphasized that $+Q_{ox}$ creation is uniform before SBD due to uniform FN stress. After SBD, $+Q_{ox}$ creation is localized at the SBD spot and thus the device has a non-uniform Vt distribution along the channel. Unlike the pMOSFET, the nMOSFET does not have Vt variation even after HBD (Fig. 5). This result is consistent with the findings by others [3]. The reason is that negative oxide charge creation in such thin gate oxide (20Å) is negligible. Fig 6. shows the noise increase ratio versus Vt shift in the pMOSFET. The dashed line in the figure indicates SBD. Apparently, the noise increases slowly in the stage of uniform charge creation (before SBD) and arises sharply after SBD due to non-uniform charge creation.

Two Region Model of Noise Degradation

Fig 7. shows the diagram of local oxide charge distribution after SBD in the pMOSFET. The breakdown position (either in the channel or in the gate and source/drain overlap region) is examined by using the method given in [4]. Table in Fig. 7 shows the ratio of Id/(Is+Id) before and after SBD. The moderate change of the ratio Id/(Is+Id) implies that the breakdown spot is in the channel [4], as illustrated in Fig. 7. A two-region model is used to explain the noise degradation due to localized charge creation. Region 1 in Fig. 7 represents the SBD spot while region 2 is the rest of the channel. The input referred noise power spectrum density for a two-region MOSFET can be modeled in Fig. 7 [5]. Due to non-uniform positive charge creation after SBD, the drain current flicker noise is greatly increased.

The channel width effect on SBD enhanced flicker noise degradation in pMOSFETs is shown in Fig 8. The noise degradation is relatively small in a larger gate width device. The qualitative model to explain the channel width dependence is given in Fig. 9.

Conclusion

The significance of oxide SBD to drain current flicker noise in ultra-thin oxide CMOS devices has been evaluated. We have shown that hole traps in pMOSFETs are easier to be created than electron traps in nMOSFETs. A small gate width pMOSFET suffers from SBD enhanced noise degradation most due to non-uniform positive oxide charge creation.

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Reference

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[3] E. Wu et al., *IEEE IEDM Tech. Digest*, P.187 1998
[4] Robin Degraeve et al., *IEEE IRPS*, p.360, 2001
[5] M.H. Tsai et al, *IEEE Trans. Electron Dev.*, p.2061, 1994

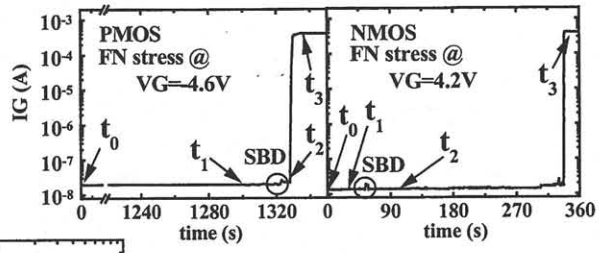


Fig1. PMOS/NMOS (W/L=1μm/0.12μm, t_{ox}=20Å) IG-time characteristics during FN stress. The flicker noise for both devices was measured at four time points : t_0(fresh), t_1(pre-SBD), t_2(post-SBD) and t_3(HBD).

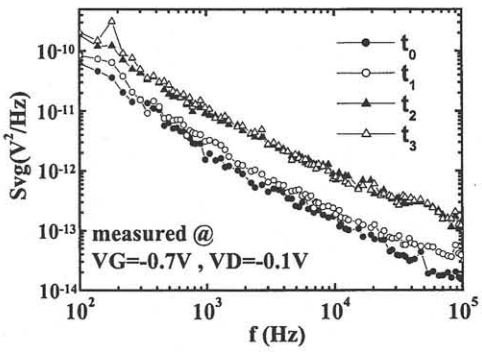


Fig2. PMOS(W/L=1μm/0.12μm, t_{ox}=20Å) noise characteristics measured at t_0(fresh), t_1(pre-SBD), t_2(post-SBD) and t_3(HBD).

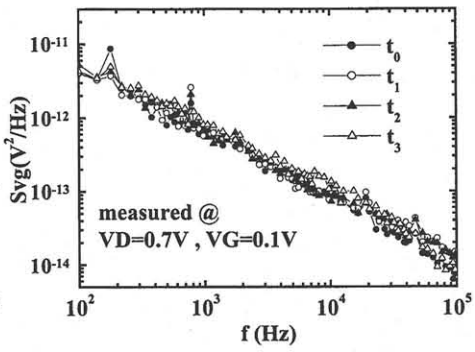


Fig3. NMOS (W/L=1μm/0.12μm, t_{ox}=20Å) noise characteristics measured at t_0(fresh), t_1(pre-SBD), t_2(post-SBD) and t_3(HBD).

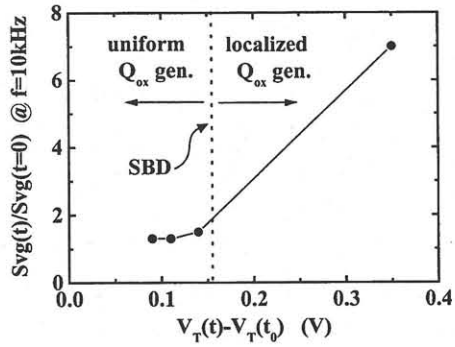


Fig6. Flicker noise increase ratio ($S_{vg}(t)/S_{vg}(t_0)$) at f=10kHz versus threshold voltage shift (Vt(t)-Vt(t_0)) for the PMOSFET (W/L=1μm/0.12 μm) during stress.

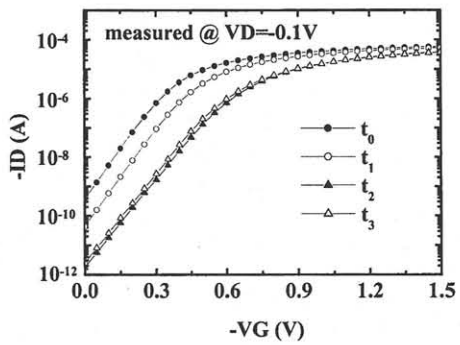


Fig4. PMOS (W/L=1μm/0.12μm, t_{ox}=20Å) ID-VG characteristics during FN stress (stress bias : VG=-4.6V).

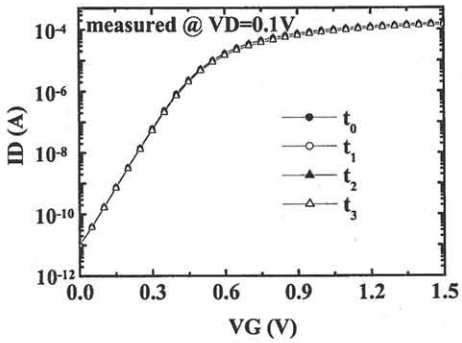
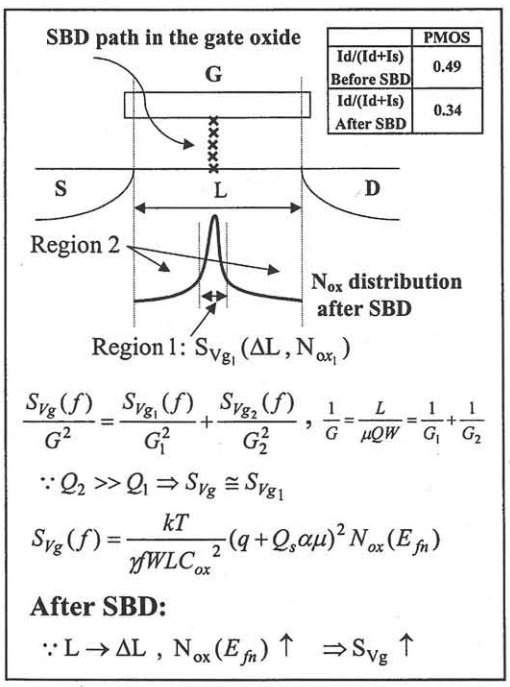


Fig5. NMOS (W/L=1μm/0.12μm, t_{ox}=20Å) ID-VG characteristics during FN stress (stress bias : VG=4.2V).



$$\frac{S_{Vg}(f)}{G^2}=\frac{S_{Vg_1}(f)}{G_1^2}+\frac{S_{Vg_2}(f)}{G_2^2},\quad \frac{1}{G}=\frac{L}{\mu QW}=\frac{1}{G_1}+\frac{1}{G_2}$$

$$\because Q_2 >> Q_1 \Rightarrow S_{Vg} \cong S_{Vg1}$$

$$S_{Vg}(f)=\frac{kT}{\gamma f WLC_{ox}{}^2}(q+Q_s\alpha\mu)^2 N_{ox}(E_{fn})$$

After SBD:

$$\because L \rightarrow \Delta L\ ,\ N_{ox}(E_{fn}) \uparrow \quad \Rightarrow S_{Vg} \uparrow$$

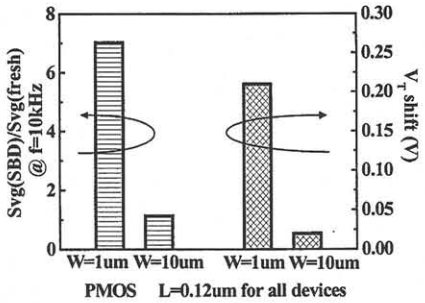
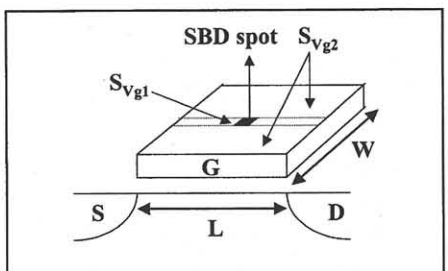


Fig8. PMOS(W=10um and 1um) noise (f=10kHz) increase ratio and Vt shift after device SBD.

Fig7. The diagram of oxide charge distribution and two region model. Current ratio before and after soft breakdown (measure @ VG=1.5V) is also shown. Region 1 is the SBD region, and region 2 is the rest of the channel. The two region can be thought as two PMOSFETs in series. (Q: channel charge , N_{ox} : oxide trap denisty)



$$S_{Id}=S_{Id_1}+S_{Id_2}$$

$$\Rightarrow g_m^2 S_{Vg}=g_{m_1}^2 S_{Vg_1}+g_{m_2}^2 S_{Vg_2}$$

For a smaller W

$\Rightarrow$ **S_{Vg_1} dominant**

$\Rightarrow$ **a larger S_{Vg} increase**

Fig9. The diagram to illustrate the gate width effect on SBD enhanced noise degradation. The SBD MOSFET can be considered as two pMOSFETs in parallel. Transistor 1 includes the SBD region and transistor 2 represents the rest of the gate width.