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Novel Deuterated Highly Reliable SiO_2 by SiD_4 Poly-Si Gate Electrode

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Introduction

It has been reported that deuterium incorporation into gate oxides is effective for the reliability improvement of SiO_2 [1-3]. Our previous work showed that the deuterium pyrogenic oxidation and the deuterated poly-Si deposition improve the stress-induced leakage current (SILC), compared with the conventional wet oxidation and poly-Si deposition [4].

For further application of the deuterium effect for ultra-thin gate oxides, we have tried to develop a novel fabrication process for highly reliable SiO_2. As a result, by utilizing SiD_4 poly-Si and the appropriate annealing process, we found that SILC suppression can be realized by the deuterium incorporation into SiO_2, even for dry gate oxides.

Experiment

The devices used in this study were MOS capacitors fabricated on n-type Si (100) substrates. Dry and wet gate oxides were grown at 850 °C. The thickness of gate oxides was around 5.5 nm both for dry and wet oxides. Poly-Si gate electrodes were deposited by use of the conventional monosilane (SiH_4) or the deuterated monosilane (SiD_4). Doping of a gate electrode was performed by phosphorous diffusion at 850 °C. At the end of the fabrication process of the test devices, hydrogen or deuterium annealing was performed at 450 °C. The areas of the measured devices were $1x10^{-3}$ cm^2. As an index of the reliability of SiO_2, we focused on SILC as a function of gate-oxide thickness (t_{OX}). Because SILC strongly depends on t_{OX}, we determined t_{OX} of all devices from the C-V measurement, before F-N stress and SILC measurement, by the sequence as shown in Fig. 1 (a). As shown in Fig. 1 (b), the SILC values were defined as the increment of the gate current at V_{GS} which was the gate voltage where the leakage current goes over 10^{-10} A/cm^2 in the initial I-V characteristics.

Results and Discussion

It is already known that a turn-around phenomenon was observed of SILC with decreasing t_{OX} under the constant current stressing [5]. Fig. 2 indicates the typical SILC distribution for wet oxide with SiH_4 poly-Si gate. As shown in Fig. 2, the turn-around of SILC was clearly observed, irrespective of the injected electron fluence (Q_{INJ}). By utilizing SiD_4 poly-Si gate, we found that remarkable SILC suppression was realized, compared with SiH_4 poly-Si. Fig. 3 shows the relationship between SILC and t_{OX}, for SiO_2 with SiD_4 poly-Si and SiH_4 poly-Si gate electrodes. The peak SILC value for SiD_4 poly-Si gate was suppressed to about 30 % compared with that for SiH_4 poly-Si gate,

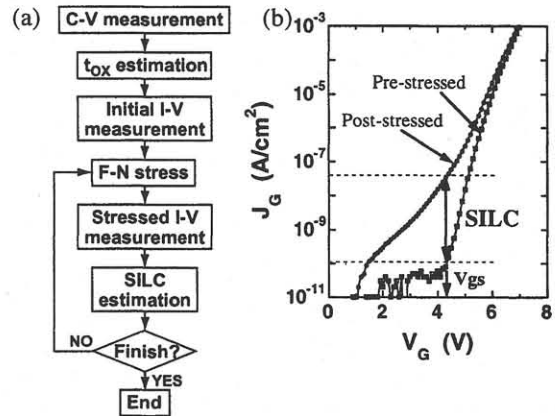

Fig. 1 Measurement method for SILC. Oxide thickness of all devices were determined by C-V measurement, before SILC measurement (a). SILC values were defined the increment of gate currents at V_{GS} after F-N stress (b).

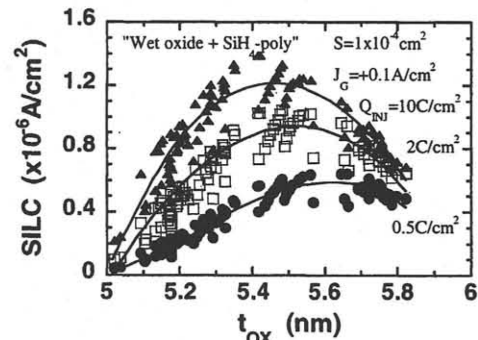

Fig. 2 SILC distribution for the conventional wet oxide with t_{OX} of around 5.5 nm. The turn-around in t_{OX}-dependence of SILC is observed, irrespective of Q_{INJ}.

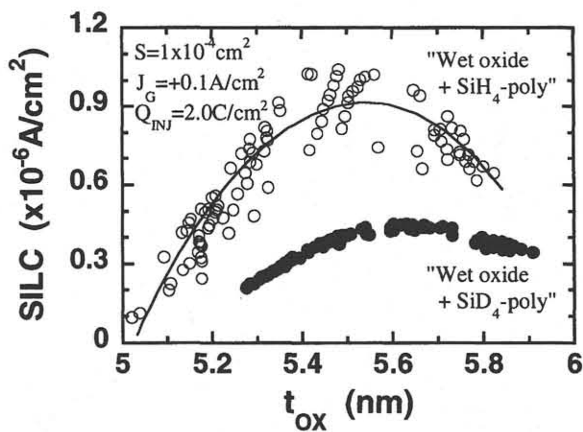

Fig. 3 SILC distributions for wet oxide, wet oxide with deuterated poly-Si gate. Note that SILC is reduced by deuterated poly-Si deposition.

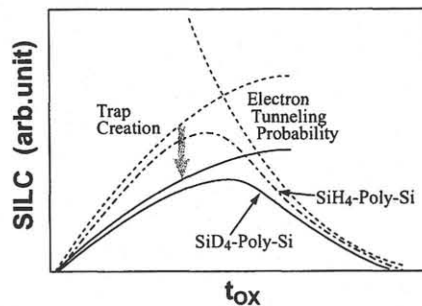

Fig. 4 Schematic diagram for the effect of deuterium incorporation on t_{OX}-dependence of SILC. It is inferred that, trap creation is suppressed by deuterium incorporation.

as shown in Fig. 3. The t_{OX} dependence of SILC was qualitatively expressed on the basis of the bond-hardening in SiO_2 network by the deuterium incorporation into gate oxide [4]. Fig. 4 indicates the schematic diagram on an interpretation of SILC suppression by the deuterium incorporation into SiO_2 for the experimental results shown in Fig. 3. It is inferred that, as same as the thick oxide case in [4], the Si-D bonds by the introduced deuterium atoms from SiD_4 poly-Si contribute to the decrease of the trap creation for the SILC generation. The deuterium incorporation effect strongly affects the SILC suppression, especially in thinner t_{OX} region under the constant current stressing (i.e. lower electron energy in thinner oxides).

Furthermore, we found that the SiD_4 poly-Si process can realize the SILC suppression even in the conventional dry oxides. Fig. 5 shows the SILC-t_{OX} relationship for dry oxides with SiD_4 poly-Si and SiH_4 poly-Si. As clearly shown in Fig. 5, the SILC values for SiD_4 poly-Si were dramatically suppressed compared with that for conventional SiH_4 poly-Si case. The experimental result shown in Fig. 5 indicates the possibility of novel deuterium-incorporation processes for the suppression of SILC in ultra-thin gate dielectrics. Though the simple deuterium-gas annealing is not effective for the SILC suppression, the appropriate deuterium incorporation into gate oxides is expressed to be effective of the SILC suppression. This message is very important for the fabrication process of ultra-thin oxynitride and future high-k gate dielectrics.

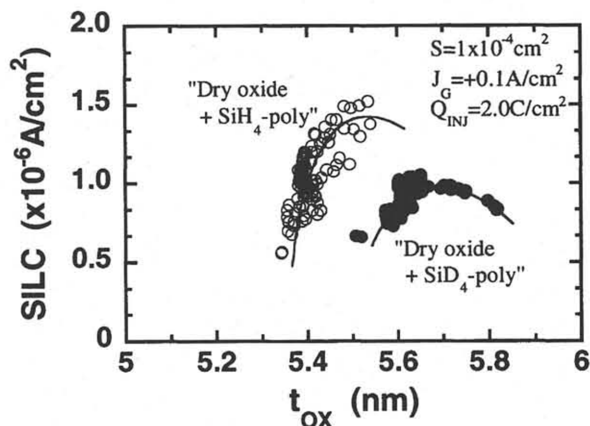

Fig. 5 SILC distribution for dry oxide and dry oxide with deuterated poly-Si gate. It was found that SILC of dry oxide is also improved by deuterated poly-Si deposition.

Conclusion

For realization of highly reliable ultra-thin gate oxides, we investigated the deuterium-incorporation process by utilizing SiD_4 poly-Si gate electrode. It was found that the suppression of SILC is observed for both dry and wet oxides, in thin oxide region. The new finding that the deuterated gate oxides excepting the deuterium wet oxides are effective for the SILC suppression will be important for the fabrication process of future gate dielectrics, and for better understanding on the mechanism of dielectrics reliability.

References

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