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Influences of Gate-edge Structure on Electric Field Strength in MISFETs with High-k Gate Dielectrics

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Abstract
It is shown that electric field strength is strongly affected by MISFETs' structure around gate-edge with high-k gate dielectrics. An explanation of this phenomenon is given with physical considerations. A new structure is proposed to reduce electric field strength.

1. Introduction
As demand for high-speed and low-power operation increases, device feature size is reduced and power supply voltage is lowered [1,2]. According to this trend, gate dielectrics are being thinned and it is estimated that they will be 1 nm for 35 nm MOSFETs [3]. In order to avoid the drastic leakage current increase that is inherent in SiO_2 gate dielectrics, high-k materials for gate dielectrics are being intensively investigated [4]. In MISFETs with high-k gate dielectrics, it is foreseen that gate-edge structure affects electric field around it, because there exists a discontinuity in dielectric constant as schematically shown in Fig. 1. We investigated the electric field using 2-dimensional simulation and found that it is influenced strongly by the location of the sidewall/gate dielectric interface relative to the gate electrode edge. We also propose a new device structure based on a consideration on the physical reasons for the phenomena.

2. Simulation and its Results
Figure 1 schematically shows a device structure in simulation. This is a 35 nm n-MISFET with a 5-nm thick gate dielectric having a dielectric constant of 19.5. A dielectric constant of the passivation layer is 3.9. Δ represents the distance between the sidewall/gate dielectric interface and gate electrode edge. Gate-edge corners (circle in Fig. 1) are assumed to be rectangular: Rounding of the corner is considered to be difficult for metal gate. Moreover, severe bird's beak enchroachment by the post-oxidation after gate-RIE has been reported for HfO_2 MISFETs [5]. Grid size near gate-edge was chosen to be 0.1 nm. Electric fields were simulated at $V_S = V_{SUB} = 0$ V and $V_G = V_D = 0.6$ V. Figure 2 shows profiles of electric field at the top surface of gate dielectric in the case $\Delta = 0$ and $V_D = 0$ and 0.6 V. It is seen that electric field is extremely high only within a few nm from gate-edges. In the case $V_D = 0$ V, electric field strength in the part indicated by a bracket agrees with that of simple parallel plate approximation. Figure 3 shows dependences of electric field strength at the surface of gate dielectric at gate-edge ($x = 0$) on Δ for 2 cases of k with an EOT of 1 nm. Here, positive/negative Δ means that gate dielectric is longer/shorter than a gate electrode (insets to Fig. 3). It is seen that electric field is the lowest for the case in which edges of gate dielectrics coincide with gate-edges and that it increases rapidly as edges of gate dielectrics are located away from gate-edges. In the case that Δ is positive, electric field becomes as high as 4 MV/cm for $k = 19.5$, which is 1% TZDB voltage in Weibull distribution for ZrO_2 [6]. In the case that Δ is negative, electric field is lower than in the case of positive Δ.
Figure 4 shows equipotential curves around gate-edge for $\Delta = 0$ and 5 nm. It is clearly seen that contour density around gate-edges is much higher, i.e., electric field strength is much higher, in the case $\Delta = 5$ nm than in the case $\Delta = 0$ nm.

3. Physical Reasons for the Dependence
Figure 5 schematically shows magnified views around gate-edges. At the interface between 2 materials of different dielectric constants, charge corresponding to their polarization difference is induced by electric field. Suppose that gate electrode is positively biased. Electric fields have horizontal components near gate-edges (arrows in Fig. 5), which induce positive charge on side surfaces of gate dielectrics. Since positive charge increases electrical potential around it, this reduces electric field. In the case of $\Delta = 0$, the amount of induced charge is the maximum and the distance between the charge and gate-edges is the minimum, resulting in the largest field suppression. Electric field increases as edges of gate dielectric are located away from gate-edges, due to the decrease in the above suppression mechanism. Contrary to the 2 cases ($\Delta = 0$, $\Delta < 0$), charge is induced both on top and side surfaces in the case of $\Delta > 0$ (Fig. 5(c)). It should be noted that induced charge on top surfaces is negative. Hence, it enhances electric field. This is the physical reason that electric field becomes higher in the case of positive Δ than in the case of negative Δ.
Dependences in Fig.3 can be understood also in terms of the enhancement of electric field strength in low-k materials due to the continuity of D, electric flux density.

4. Reliable Gate-edge Structures
Although the most preferable Δ is 0, it is extremely difficult to realize it reproducibly. It is known from the above considerations that negative Δ is the next most preferable Δ. Furthermore, electric field is at its maximum not in high-k material but in passivation material in this case. In the case that positive Δ has to be chosen, some new structure around gate-edges is required. Considering the physical reasons, we propose a new structure in Fig. 6. Not only gate dielectrics but also gate sidewalls are made of high-k materials. When gate electrode is positively biased, positive charge is induced also on bottom and side surfaces of the sidewalls (Fig. 6(b)). This induced charge reduces electric field. Figure 7 shows dependences of electric field strength on dielectric constant of sidewalls with sidewall thickness as a parameter. As the dielectric constant increases from 3.9 to 39, electric fields decrease to about half. As sidewalls become thinner, the induced charge on side surfaces of sidewalls increases and the distance between it and gate-edge decreases, resulting in larger field suppression effect. Hence, electric field decreases with thickness of sidewalls.
In the structure shown in Fig. 6(a), the increase in capacitance between gate and source/drain (C_{OV}) and high-k related phenomena such as ZIBL, FIBL, and FIBS [7-9] must be considered. Figure 8 shows dependences of C_{OV} on dielectric constant of sidewalls with sidewall thickness as a parameter, indicating that it increases slightly with dielectric constant of sidewalls in thin sidewall cases. In order to clarify an effect of high-k related phenomena, threshold voltage differences between devices in Fig. 6(a) and the device in Fig. 1 with $\Delta = 0$ are studied, as in Fig. 9. Differences are a few times 0.1 mV in all cases. Hence, the above phenomena are not serious. Therefore, the structure in Fig. 6(a) with

properly chosen design parameters effectively suppresses electric field strength around gate-edges, neither increasing parasitic capacitance nor enhancing high-k related phenomena.

5. Summaries and Conclusion

It has been shown that using high-k material as gate dielectrics in MISFETs induces a new problem related to electric field enhancement. Therefore, gate-edge structure in high-k gate dielectric MISFETs must be carefully designed from the viewpoint of avoiding this problem.

References

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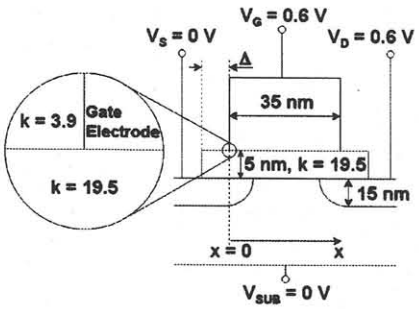

Fig.1 A schematic picture of a device in the simulation.

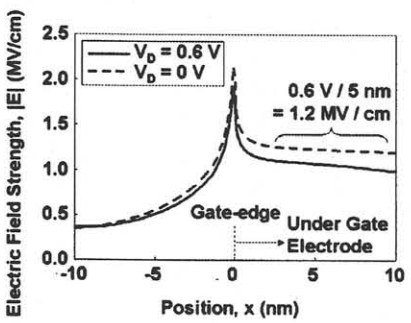

Fig.2 Profiles of electric field at the top surface of gate dielectric.

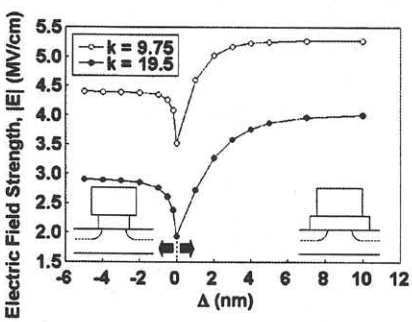

Fig.3 Dependences of electric field strength on Δ.

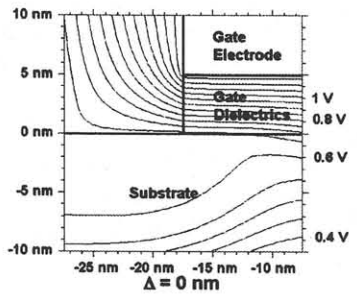

Fig.4(a) Equipotential curves around gate-edge for the case of Δ = 0 nm.

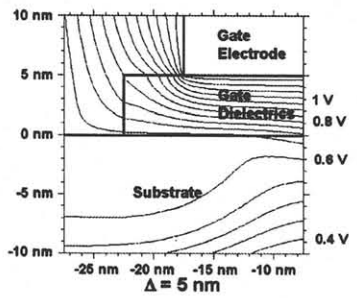

Fig.4(b) Equipotential curves around gate-edge for the case of Δ = 5 nm.

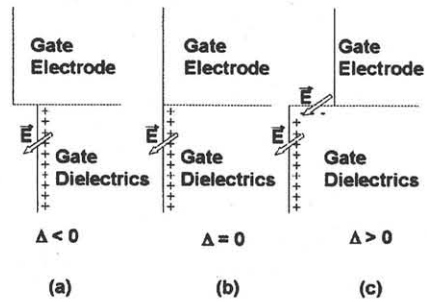

Fig.5 Magnified views of gate-edge for (a) Δ < 0, (b) Δ = 0, and (c) Δ > 0.

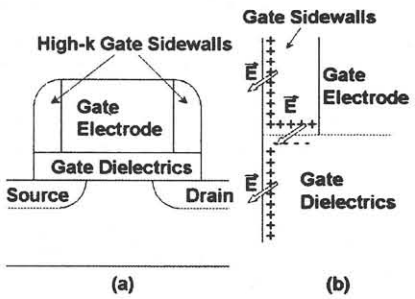

Fig.6 (a) A new structure for reduction of electric field. (b) A magnified view of gate-edge.

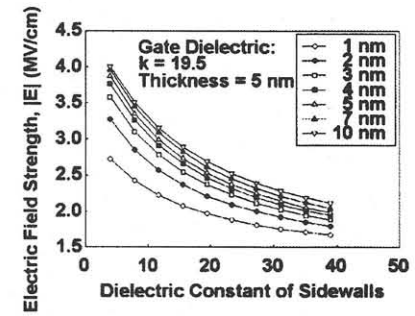

Fig.7. Dependences of electric field strength on dielectric constant of gate sidewalls with sidewall thickness as a parameter.

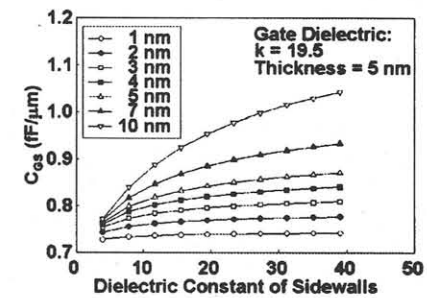

Fig.8 Dependences of capacitance between gate and source on dielectric constant of gate sidewalls with sidewall thickness as a parameter.

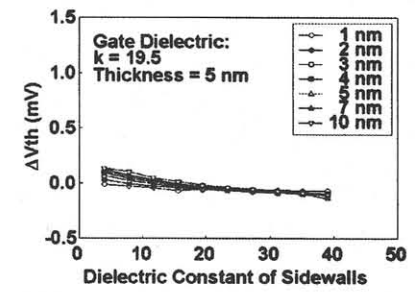

Fig.9 Dependences of threshold voltage difference on dielectric constant of gate sidewalls with sidewall thickness as a parameter.