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SiO_2/Si Suboxide Characteristics of Ultra-Thin Gate Oxides Prepared by Room Temperature Anodic Oxidation and Rapid Thermal Oxidation

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1. Introduction

Ultrathin SiO_2 under 20Å will be adopted as a gate dielectric of CMOS transistor for sub-0.1μm technology node. It is known that oxides below 15Å thickness can result in high leakage current. Generally, the SiO_2/Si interface is not perfectly flat, a transition region (suboxide region, SiOx, x<2) exists within the interfacial region of about 30 Å [1]. Since the suboxide layer may broadly distribute in this ultrathin region, an atomic scale variation in the effective oxide layer can lead to an order of magnitude variation in local tunneling current. It is therefore of importance to improve the suboxide quality.

In this work, room temperature anodic oxidation and conventional rapid thermal oxidation (RTO) are used to study ultrathin SiO_2 layers. The anodic oxide presents less leakage characteristic and less barrier height lowering effect than RTO SiO_2. A sharper transition from SiO_2 to Si was observed for anodic oxides.

2. Experiment

Prior to anodization, p-Si wafers were treated with standard RCA. For anodic oxidation, DC 15V superposed with an AC 5V was applied at the wafer using DI water as electrolyte, then performed with RTA annealing. The schematic diagram of the system is shown in Fig.1. Also, conventional SiO_2 prepared by RTO at 850℃ was also fabricated for comparison. All dielectrics were characterized by AES, XPS and Ellipsometer. In addition, C-V and J-V were also utilized to analyze the electrical characteristics. The oxide thickness is obtained from C-V measurement, considering the series resistance and quantum mechanical effects [2], [3].

3. Results and Discussion

In Fig. 2(a), AES depth profile of 1000Å SiO_2 is shown to a have a stoichiometric distribution of Si and O atoms in the bulk. In addition, the profiles of 40 Å SiO_2 prepared by RTO and anodization are shown in Fig.2 (b). We can see that the Si, O concentrations present relative sharper distributions in the anodic SiO_2. Also, the suboxide thickness is estimated to be 32Å. XPS Si 2p spectra with 40Å SiO_2 grown by (a) RTO and (b) anodic oxidation are shown in Fig.3. For the silicon oxide, four different bonding configurations were admitted, i.e., Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+}, which have distinguishable energy shifts relative to the binding energy of the bulk silicon, i.e., 1.0, 1.8, 2.7, and 3.5 eV, respectively [4]. It is obviously observed that thermal grown RTO SiO_2 contains more suboxide rearrangements in the transformation from Si to SiO_2. It is believed that more imperfect bonding could occur during the reaction of Si and oxygen mass under high temperature oxidation. Anodic oxide shows much sharper transition in suboxide region due to room temperature layer-by-layer reaction of OH^- and Si.

Fig. 4 shows the leakage current comparison of RTO and anodic SiO_2. The anodic SiO_2 presents an order lower leakage current than RTO one, indicating less suboxide existing could effective reduce the local thinning induced tunneling current. Also, TZDB characteristic comparison is shown in Fig. 5. Higher breakdown field is observed for the anodic SiO_2. It is believed that less weak suboxide bonding rearrangement would enhance the anodic oxide to suffer higher breakdown field.

It was reported that the suboxide (SiO_x) barrier height dependents on the x value [5]. Higher x value could induce the higher barrier height. Fig. 6 shows barrier height roll off characteristics of RTO and anodic SiO_2 due to suboxide effect. The barrier height values were extracted from the F-N plots with $m_{ox} = 0.42m_o$ as shown in the insets. It is observed the anodic SiO_2 exhibits a higher barrier height characteristic than RTO SiO_2 under the same oxide thickness. Here, we proposed a model to describe the barrier roll off phenomenon due to suboxide effect as shown in Fig. 7. Less unsound bonding exists in the oxide layer would lead to a more perfect barrier shape. Therefore, room temperature anodic oxidation process can prepare a more perfect ultra-thin SiO_2 layer via the control of less suboxide existence.

4. Conclusions

Conventional thermal grown SiO_2 and anodic SiO_2 comparison is studied in this work. Anodic SiO_2 contains more oxygen atoms and less suboxide arrangement in the oxide layer, hence a better electrical characteristic. Also, suboxide induced barrier lowering is also discussed due to suboxide effect. With respect to the thermal oxidation, anodic SiO_2 can be an alternative for gate dielectric.

Acknowledgements

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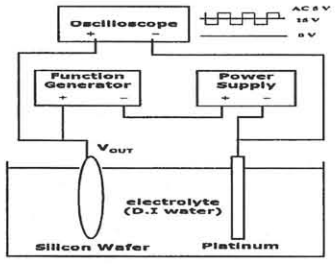

Fig. 1 Schematic diagram of anodic oxidation system.

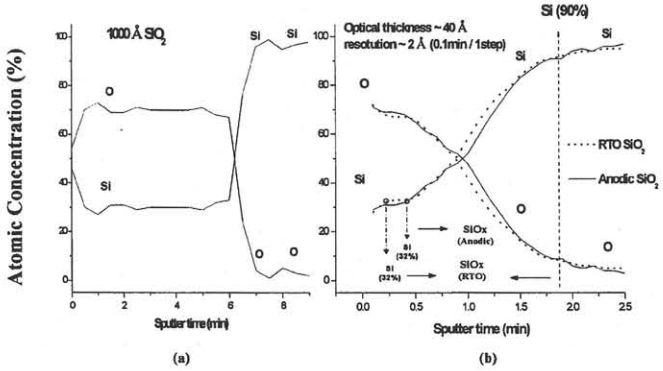

Fig. 2 AES depth profiles of (a) 1000Å SiO_2 and (b) 40Å RTO and Anodic SiO_2.

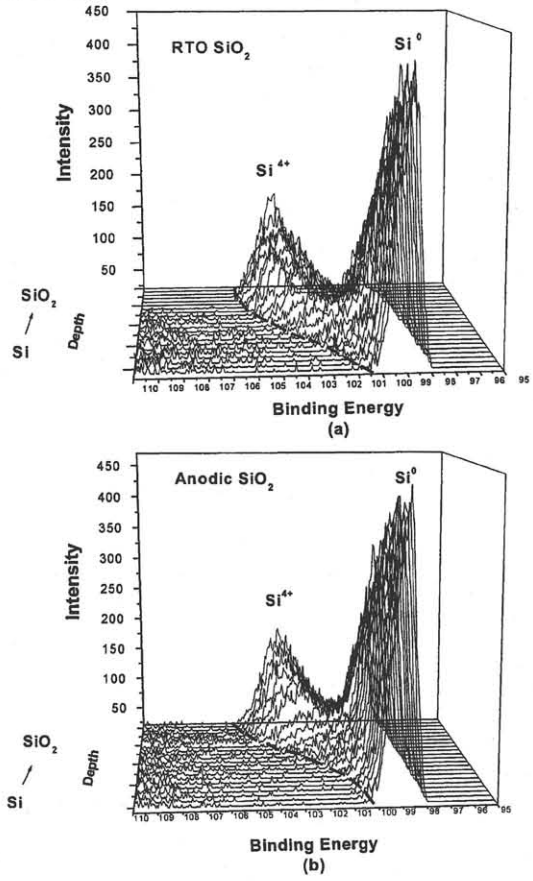

Fig. 3 Evolution of XPS Si 2p spectra with 40Å SiO_2 grown by (a) RTO and (b) room temperature anodic oxidation.

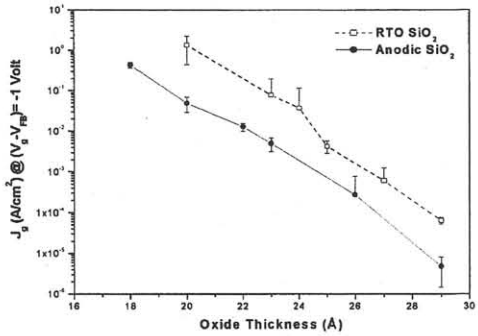

Fig. 4 Gate leakage current densities versus oxide thickness of RTO and anodic SiO_2 samples with a gate bias at $Vg-V_{FB} = -1V$.

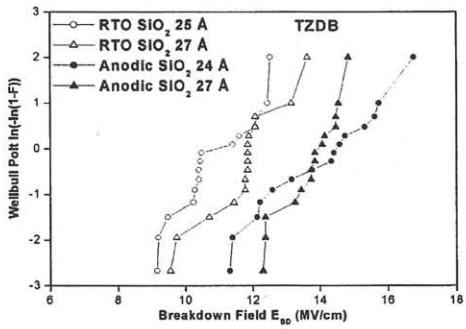

Fig. 5 Weibull plot of TZDB characteristic for RTO and anodic SiO_2 samples.

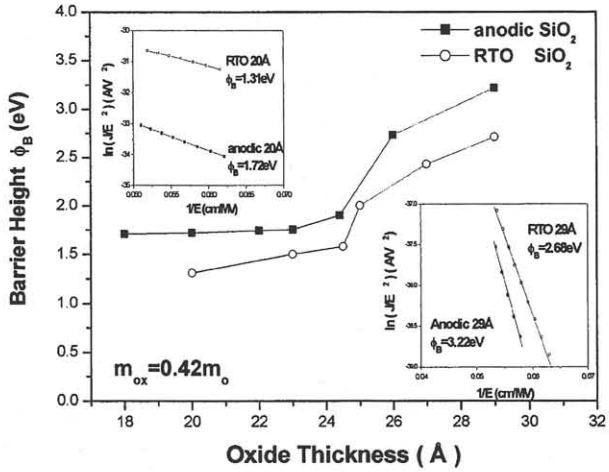

Fig. 6 Barrier height versus oxide thickness of RTO and anodic SiO_2. F-N plots of 20Å and 29Å oxide thickness are inserted in the figure.

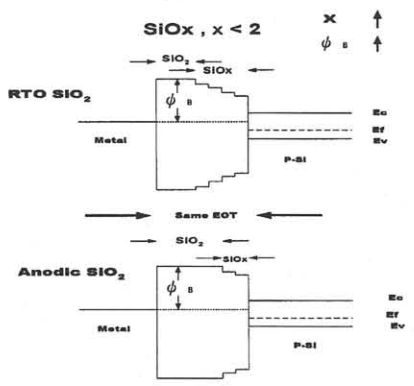

Fig. 7 Models of suboxide induced barrier lowering of (a) RTO and (b) anodic SiO_2.