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Critical Materials Issues for High-k Gate Dielectric Integration

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1. Introduction

The integration of new high-k gate dielectric materials into advanced planar CMOS technology presents several significant challenges [1]. Moreover, the introduction of these materials is expected to occur at an unprecedented pace to meet industry technology forecasts and will therefore mandate a rapid correlation of physical characterization with electrical performance. Although recent research has emphasized the search for a material that yields a suitable (higher) dielectric constant relative to SiO_2, a more important problem is the integration of *any* new dielectric material candidate in *existing* CMOS flows in a cost-effective manner, given industry roadmaps. These integration issues include thermal stability, etching, control of phase segregation, dopant penetration, gate electrode compatibility, and many others that will influence the resultant electrical properties [2].

This talk will examine several of these integration challenges that must be addressed for successful high-k gate dielectric integration.

2. Thermal Stability

The extent of impurity incorporation from constituent species in the gate dielectric into the Si channel region is an important example. Significant impurity incorporation ($>10^{16}/cm^3$) into the Si channel region of CMOS devices is well known to degrade mobility. To examine the possibility of such interdiffusion, 5 nm Zr-silicate and Hf-silicate uncapped films were annealed in N_2 at various temperatures and times. These films were then chemically removed to permit depth profile characterization using multicrater Time-of-Flight Secondary Ion Mass Spectrometry (ToFSIMS) methods.

Comparison of Zr-silicate and Hf-silicate

As seen in Fig. 1, aggressive thermal annealing Zr-silicate results in the interdiffusion of Zr with the Si substrate [3]. Extrapolation of the impurity depth profiles with a simple diffusion models indicates a diffusion coefficient $D_0 \sim 2\times10^{-15}$ cm^2/s and that the resultant impurity concentration in the near surface region is above acceptable limits ($\sim10^{16}/cm^3$) for relevant rapid thermal annealing thermal budgets (~1050°C, ~5 s).

In contrast, Hf interdiffusion from Hf silicate is below ToFSIMS detectible limits after similar annealing conditions [4]. Fig. 2 shows results for ToFSIMS depth profiles for Hf in Si after annealing and subsequent etch removal in two modes of data acquisition: single crater sputtering vs. multicrater methods. It is seen that multicrater profiles are required to accurately determine the depth profile of impurities in the near surface region.

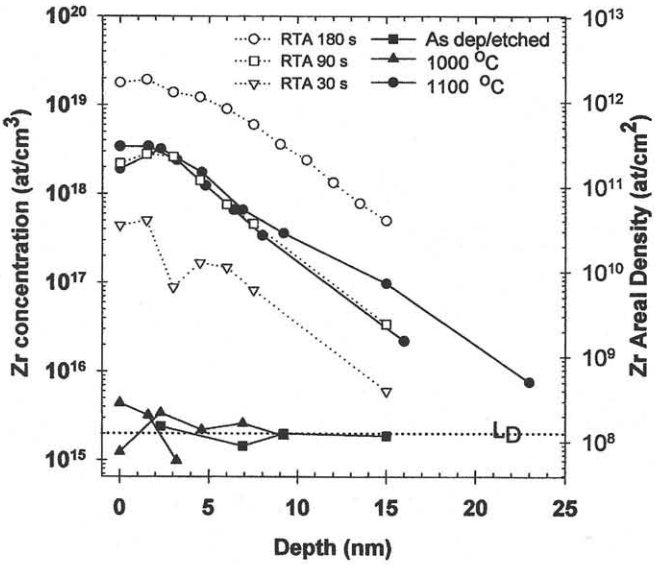

Fig. 1 Multicrater ToFSIMS Zr depth profiles in Si after annealing and etching 50Å Zr-silicate films.

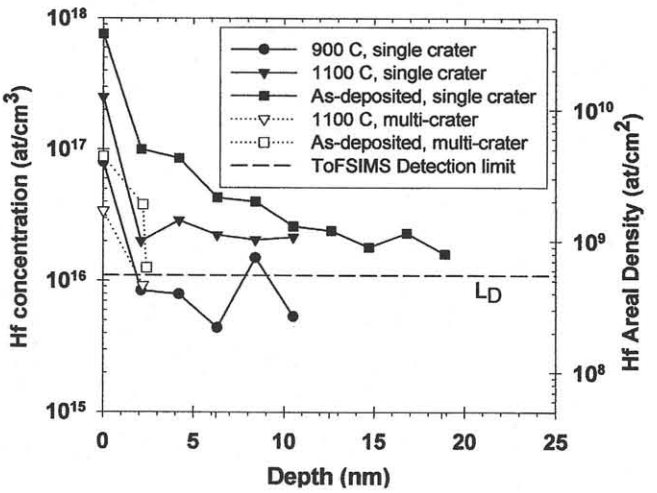

Fig. 2 ToFSIMS Hf depth profiles in Si after annealing and etching 50Å Hf-silicate films. The multicrater technique avoids spurious Hf knock-on redistribution into the bulk.

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These results suggest that Hf-based dielectrics appear to provide enhanced thermal stability over Zr-based dielectrics for conventional gate dielectric integration process flows.

3. Dopant Diffusion

An equally important issue is the control of dopant outdiffusion from doped polycrystalline Si gate electrodes through the gate dielectric into the Si channel. Successful application of oxide-based alternative gate dielectric materials in the near term will require materials engineering, such as nitridation [5], to inhibit dopant diffusion similar to that required for SiO_2 [6]. To examine this issue, doped poly-Si capped Hf-silicate films were annealed to examine the extent of dopant penetration into the underlying Si substrate. The poly-Si cap and the dielectric were then subsequently etched to facilitate dynamic SIMS analysis from the "front" side of the sample.

B diffusion through Hf-silicate

Fig. 3 shows the SIMS depth profiles of B into the underlying n-type Si substrates clearly showing significant B penetration after anneals at 1050°C. The concentration of Hf in these Hf-silicate films is 14 at.% and is thus sufficient to result in the formation of nanocrystalline regions (Fig. 4). The grain boundaries associated with these regions are expected to enhance dopant diffusion through the dielectric. In these studies, control of the film morphology (nanocrystalline vs. amorphous), which is dependent upon control of the Hf concentration in the Hf silicate films, appears to be an important consideration.

The incorporation of N within these alternate dielectric materials [5] is also expected to inhibit dopant diffusion and preserve some margin to maintain film amorphicity throughout the thermal processing associated with conventional CMOS flows [7]. We will present studies examining the impact of nitridation on B, P and As dopant diffusion through Hf-silicate films.

4. Conclusions

Several high-k gate dielectric candidates are now under investigation around the world. Although some materials exhibit promise in gate dielectric applications, studies on the materials integration aspects must be emphasized for successful, near-term insertion for scaled CMOS.

Acknowledgments

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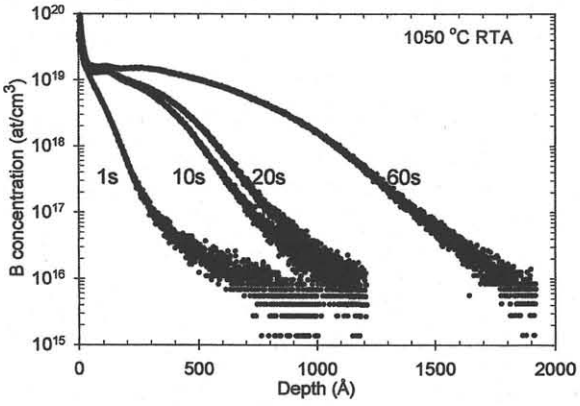

Fig. 3 SIMS depth profiles of B in n-type Si from annealed Hf-silicate films

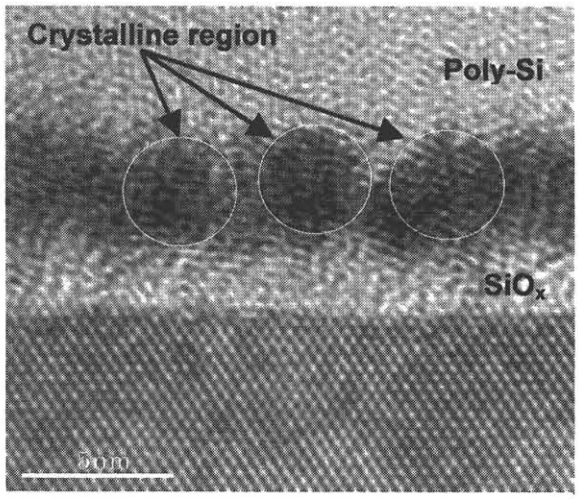

Fig. 4 HRTEM of poly-Si capped Hf-silciate film after RTA at 1050 C for 60 s.

References

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