# Impact of Hf metal pre-deposition in CVD- and PVD-HfO<sub>2</sub> dielectrics

Kazuhiko Yamamoto<sup>1</sup>, Masayuki Asai<sup>2</sup>, Shigenori Hayashi<sup>1</sup>, Sadayoshi Horii<sup>2</sup>,

Masaaki Niwa<sup>1</sup>, and Hironobu Miya<sup>4</sup>

<sup>1</sup>ULSI Process Technology Development Center, Matsushita Electric Industrial Co., Ltd.

19, Nishikujo-Kasugacho, Minami-ku, Kyoto, 601-8413, Japan

Phone:+81-75-662-8994, Fax:+81-75-662-8995, E-mail:yamamoto@krl.mec.mei.co.jp

<sup>2</sup>Semiconductor equipment system laboratory, Hitachi Kokusai Electric Inc.

2-1 Yasuuchi, Yatsuo-Machi, Nei-gun, Toyama, 939-2393, Japan

### 1. Introduction

High- $\kappa$  gate dielectrics have been extensively studied with much attention focused on HfO<sub>2</sub> and ZrO<sub>2</sub>[1,2]. However, there have been some difficulties in preparing these thin films by chemical vapor deposition (CVD) and physical vapor deposition (PVD). A post -deposition annealing (PDA) is required to densify CVD-HfO<sub>2</sub> removing impurities (Cl, hydrogen, carbon and H<sub>2</sub>O)[3,4]. CVD growth in oxidizing ambient and PDA process cause the thick interfacial layer growth. Although PVD-HfO<sub>2</sub> is no contaminated with impurities like CVD-HfO<sub>2</sub>, energetic species are likely to react with Si substrates, leading to a thick interfacial layer [5-8]. Both deposition techniques will make the thick interfacial layers with low permittivity, leading to increase an effective oxide thickness. In this paper, we will demonstrate the EOT reduction of CVD- and PVD-HfO<sub>2</sub> capacitors with acceptable lower leakage current by means of pre-deposition of Hf metal layer.

#### 2. Experimental procedure

Figure 1 shows the fabrication process of MOS capacitor with TiN/HfO<sub>2</sub>/Hf/RTN-SiN/p-type Si stack. PVD-Hf metal pre-deposition on nitrided (<1nm) Si substrates prior to CVD- or PVD-HfO<sub>2</sub> deposition (0-2nm) was performed by sputtering Hf target in Ar. CVD-HfO<sub>2</sub> was grown by metal organic CVD using tetrakis(1-1-dimethyl-2-methoxy-Hf)(Hf[OC(CH<sub>3</sub>)<sub>2</sub>CH<sub>2</sub> OCH<sub>3</sub>]<sub>4</sub>) and plasma-oxygen. PVD- HfO<sub>2</sub> was prepared by reactive sputtering from Hf metal target in Ar/O<sub>2</sub>. PDA of the HfO<sub>2</sub>/Hf was performed at 650 °C for 15 min in N<sub>2</sub>. After the HfO<sub>2</sub>/Hf deposition, TiN layer was grown by CVD at 650 °C and were defined by photolithography and etching to form gate electrode of MOS capacitor. The capacitance equivalent thickness (CET) of HfO<sub>2</sub> was obtained from capacitance value at Vg = -3 V.

#### 3. Results and Discussion

#### A. CVD-HfO<sub>2</sub>

Figure 2 shows the CET and leakage current density at -1V (Jg) dependence of CVD-HfO<sub>2</sub>/PVD-Hf stack capacitors on the pre-deposited Hf metal thickness. The CVD-HfO<sub>2</sub> thickness is fixed to 3.4 nm. With decreasing the Hf metal thickness, the CET decreases due to the thinning of physical thickness. However, the CET reduction is deteriorated to approximately 1.6 nm for thinner Hf metal thickness regime (<~0.5 nm). Jg of the CVD-HfO<sub>2</sub> without Hf metal layer is three-orders of magnitude larger than that of Hf metal pre-deposited samples. To illustrate the effect of Hf metal pre-deposition, the CET plots are compared in Fig. 3. The solid triangles represent the CET for CVD-HfO<sub>2</sub> films without Hf metal layer. In the case of CVD-HfO<sub>2</sub> on Hf metal layer, total thickness is calculated as  $T_{total} = T_{Hf} \ge 1.62 + 3.4$  (nm), owing to the assumption that the thickness of HfO<sub>2</sub> increases by 1.62 times from that of Hf metal layer when Hf metal is completely oxidized. As can be expected from the intersection in the y axis, the interfacial layer thickness of HfO<sub>2</sub>/Hf stack capacitors is smaller than that samples without Hf metal layer. Note that HfO<sub>2</sub>/Hf capacitors grown at lower temperatures revealed much smaller CET. We speculate that the difference of slope, permittivy, reflects the film quality. Figure 4 shows the CET versus Jg at Vg = -1 V of CVD-HfO<sub>2</sub>/Hf capacitors. Jg of HfO<sub>2</sub>/Hf stack capacitors at the same CET value is smaller than that of samples without Hf metal layer. These results indicate that Hf metal pre-deposition suppresses the increase of the interfacial layer thickness (hence reduces the CET) and improves the film quality with low leakage current.

#### B. PVD-HfO<sub>2</sub>

Figure 5 shows the CET and Jg dependence of PVD-HfO2/PVD-Hf capacitors on the pre-deposited Hf metal thickness. The sputtering conditions of HfO2 films are the same for all samples, where the HfO2 thickness is fixed to 1.3 nm. When HfO<sub>2</sub> film is directly deposited on Si (0nm), the CET is around 2.6 nm, which is thicker than the HfO<sub>2</sub> thickness (1.3 nm), implying the growth of a relatively thick interfacial layer like SiO<sub>2</sub> during sputtering. It is interesting to note that the CET tends to decrease dramatically with increasing the Hf metal layer thickness and reveals minimum CET value (~1.3 nm) at an approximately 1.3 nm of pre-deposited Hf metal layer prior to the HfO<sub>2</sub> deposition, indicating that permittivity of HfO<sub>2</sub> with Hf metal is higher than that without Hf metal. In contrast, lower Jg is obtained for both thin and thick regime of Hf metal layer due to the thick interfacial layer and the thick physical thickness of HfO<sub>2</sub>, respectively.

Figure 6 shows the TEM images for as-sputtered  $HfO_2$  films on Hf metal thickness, (a) 0nm, (b) 1.3nm, and (c) 3.9nm. As seen in (a), it is clearly observed a 2.8 nm thick interfacial layer is present between the  $HfO_2$  layer and the substrate after sputtering of an 1.3 nm thick  $HfO_2$  layer. The thick interfacial layer is likely formed due to the sputtering in an  $Ar/O_2$  gas mixture. When the Hf metal layer is thin enough, the excess oxidizing species such as radical, ion, and molecule in plasma result in this interfacial layer growth by diffusing into Si substrate to form SiO<sub>2</sub> layer. Then the total CET starts to increase again with further increase of Hf metal layer is prevented by consuming the pre-deposited Hf metal into  $HfO_2$  and its silicate. This leads to a significant

reduction in the SiO<sub>2</sub> like interfacial layer thickness. Note that the  $HfO_2$  film on thick Hf metal (c) is crystallized although that on thin Hf metal (a, b) remained as an amorphous phase. From this, the simple oxidation of Hf metal was found to make the films to be crystallized, leading to the leaky films.

Figure 7 shows the CET versus Jg at Vg = -1 V of PVD-HfO2/Hf capacitors. Different slopes in Jg vs CET indicate different conduction mechanism due to the change of stack structures.

From above experiments, the pre-deposited Hf metal layer is found to be effective to block the diffusion of oxygen into Si due to the oxidation of Hf metal for both CVD and PVD growth. In PVD, oxygen radical in plasma has much oxidative than that in CVD, resulting in the thicker CET than that without Hf metal.

## 4. Conclusions

The Hf metal pre-deposition prior to Hf oxide deposition was used to modify the structure of interfacial layer to achieve a thin CET for both CVD and PVD techniques. During the growth, the oxidation of Si substrate was inhibited because the excess oxygen species are used for the oxidation of Hf metal, resulting in a thin interfacial layer with higher Hf composition. This pre-deposition technique can be applicable to most high-k materials and deposition methods.

#### References

 [1] E. P. Gusev et.al., IEDM Tech. Dig. p.451, 2001.
 [2] Y. Kim et.al., IEDM Tech. Dig. p. 455, 2001.
 [3] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, IEDM Tech. Dig. p31, 2000.

[4] Z. Zao, T. P. Ma, E. Cartier, M. Copel, and T.Tamagawa, Symp. VLSI Tech. Dig., pp. 135, 2001.
[5] A. Callegani, E. Cartier, M. Gribelyuk, H. F.

Okorn-Schmidt, and T. Zabel. J. Appl. Phys. 90, 6466, 2001.

[6] R. Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. C. Lee, Symp. VLSI Tech. Dig., pp. 15, 2001.

[7] B. H. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, IEDM Tech. Dig. 133, 1999. [8] S-H. Su, and M. Yokoyama, ECS Let., 4, F18, 2001.

