Low-cost Cu Interconnects Using Direct Patterning Process (DPP) of Photo-sensitive MSZ with Low-k, Bottom Anti-reflective layer

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Introduction

In system on a chip (SoC), multilevel interconnects consist of three tiers, local, semi-global and global wiring for decreasing the power consumption [1] (Fig.1). The process cost, however, will be boosted up for the increasing of the interconnect layers with low-k materials due to the complexity of the fabrication process. Recently, the novel low-cost process for the inter-line dielectrics (ILD) was proposed, using the direct patterning process (DPP) of methylsilsesquiazane (MSZ) by the photo-chemical reaction for EB irradiation [2]. The photosensitive low-k dielectrics enable us to reduce 30% of the total process time due to eliminating the photo resist coating, dry-etching and resist ashing (Fig.2), while several technological issues, such as the pattern shape deformation by standing-waves of UV-exposures, are pointed out as shown in Table 1.

In this paper, we propose the novel DPP of MSZ with a bottom anti-reflective dielectric layer for the future low-cost semi-global interconnects by the KrF (248nm) lithography.

Characteristic of MSZ film

The DPP of MSZ is composed of two key-processes such as the MSZ pattering and the transformation to methylsilsesquioxane (MSQ), which are based on the reaction from Si-NH to Si-OH. The UV exposure promotes the photo acid generation, weakening the Si-NH bond. The moisture treatment changes the Si-NH to Si-OH effectively. From the FT-IR spectra, the Si-OH bond was observed in the MSZ film after the UV-cure with the moisture treatment (Fig.3). In the exposed portion, Si-NH bonds are transformed to the Si-OH bonds, which are dissolved in a tetra-methyl-ammonium hydroxide (TMAH) developer. After the development, the Si-NH bonds in the unexposed portions are changed to MSQ though the Si-OH by 400 °C-annealing. Because the remnant NH-bonds degrade the film properties, the complete transformation from Si-NH to Si-OH is crucial. For example, the thermal stability of the MSQ film strongly depends on the condition of moisture treatment. A condition of high humidity over 80% at 50 °C accelerates the Si-OH formation, resulting in the high thermal stability of MSQ obtained (Fig.4). We confirmed that the MSZ film had low dielectric constant (k=2.7), high break-down strength (>3MV/cm) and high thermal stability (>400℃).

Novel direct patterning process of MSZ

The single damascene (SD) process flow was designed for Cu interconnects in Fig.5. The 300nm-thick, MSZ film was spin-coated on two kinds of substrates, which were (1) SiN/SiO₂/Si-aubstrate and (2) SiO₂/p-BCB[3]/Si-substrate, followed by the KrF exposing of 44mJ. The MSZ trench formation was carried out through the moisture treatment-1 and TMAH development. After the photo-lithography, the UV cure, the moisture treatment-2 and 400 $^{\circ}$ C-annealing were provided for the MSQ formation. The MOCVD-Cu/PVD-barrier films (Cu=600nm, Ta/TaN=15nm/15nm) were directly deposited in the trench patterns followed by PASCAL-CMP [4].

In the case of SiN/SiO2/Si-substrate (Fig.6), the standing-waves between the substrate and the MSZ surface, which was caused by the strong refraction from the underneath layers, were conspicuously observed. To reduce the refraction from the substrate, we adopted a bottom anti-refractive layer structure the SiO₂/p-BCB/Si-sibstrate (Fig.7). The trenches have flat side-walls, which coincide with the simulated shapes. Consequently, the 0.28µm width Cu interconnects was fabricated, which have the good sheet resistance (Fig.8).

Conclusions

The novel direct patterning process (DPP) with the photo-sensitive low-k dielectric MSZ (methylsilsesquiazane) was adopted to fabricate the Cu damascene interconnects using the KrF (248nm) lithography. The film has low dielectric constant (k=2.7), high break-down strength (>3MV/cm) and high thermal stability (>400°C). The UV-cure, the moisture treatment and the bottom anti-reflective layer were the key processes for the KrF-DPP. The photo-sensitive MSZ offers the low-cost process with low inter-line capacitance especially for the semi-global interconnects.

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References

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Fig.1 System on a chip multilevel interconnect architecture using three tiers of local, semi-global and global interconnects. The cost down of the semi-global process is one of the issues for multilevel interconnects.



Fig.2 Comparison of process time between the conventional spin-on low-k dielectric and the MSZ. The 30% reduction of process time is estimated in the MSZ.

90°C/60%

70°C/60%



Fig.3 FT-IR spectra of the MSZ film; (a)as deposition, (b) after UV-cure and moisture treatment. The combination of UV cure and moisture treatment change Si-NH bond to Si-OH bond effectively.

Fig.4 TDS spectra of MSZ film. The thermal stability of the MSZ film was strongly depended on the condition of the moisture treatment.

400



Fig.6 The SEM micrographs of the trench patterns of MSZ on the SiN/SiO₂/Si-substrate after the development. The standing waves between the substrate and the MSZ surface caused the non-flat side-walls.



Fig.7 The SEM micrographs of the trench patterns of MSZ after the development. The pattern shape was improved by using the bottom anti-reflective layer structure such as SiO₂/p-BCB/Si-substrate.

Table 1 Issues of direct patterning process for Cu interconnects.

Subject	Issues
Cost-effective process for Cu-interconnects	The application for Cu damascene interconnect with DPP has not demonstrated vet.
Low-k ILD properties	Thermal stability, k-value and break-down strength of the film may be degraded by the photo-sensitive property.
UV lithography (KrF)	For semi-global line using KrF, standing waves are crucial problems without the anti-reflective coating (ARC).



Fig.5 Single Cu-damascene process flow for Cu/MSZ interconnects. The moisture treatment was used for both the lithography and the MSQ formation.





100 200 300 Temp.[°C]