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Integrated High-k and Metal Gate Processing Using RTP and ALCVD™

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1. Introduction

The main challenge for advanced gate stack processing is the introduction of a new, high-k gate dielectric, first with a polysilicon gate electrode and later on with a metal electrode. Recent publications suggest that in cases of high-k dielectric integration, issues in the area of mobility degradation and charge trapping can be overcome and that high-k gate dielectrics are suitable for high performance microprocessor applications [1]. Some results on metal electrodes have been published, as well [2].

This paper discusses some of the critical processing steps in the gate-stack formation using RTP for pre- and post-deposition treatments and ALCVD for the deposition of the high-k and metal layers.

2. Experimental

All process steps discussed in this paper are executed in ASM's Gate Stack Polygon, single-wafer cluster tool, of which a layout is presented in Fig. 1. It includes 4 modules

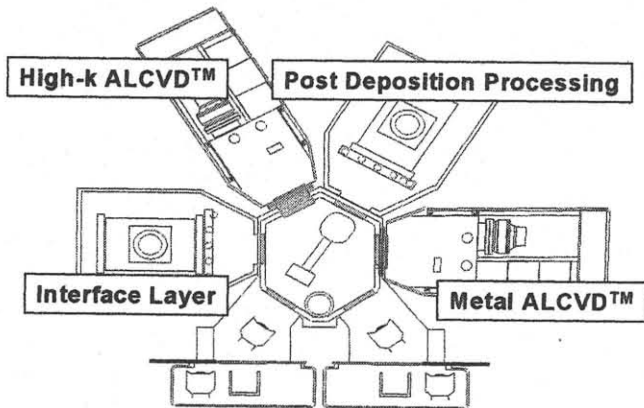

Fig. 1 Layout of the ASM Polygon™ 8200 cluster tool for high-k gate stack processing.

modules, two of which are RTP type and two are ALCVD modules. The two RTP modules are basically the same in terms of hardware and process capabilities and are derived from ASM's standalone Epsilon™ reactor for epitaxy of Si, SiGe and SiGeC [3]. Process temperature and pressure can be varied over a wide range; while a diversity of oxidation, nitridation, annealing and CVD processes are available, most of which were specifically developed for certain applications. In the gate stack application discussed in this paper, Epsilon modules are used: (1) to supply the interface layer between the Si substrate and the high-k layer; (2) to perform an optional (reactive) anneal or deposition after high-k deposition; and (3) for RTCVD of poly Si, SiGe or SiGeC for gate electrode formation. The latter two processes are combined in one module to reduce cycle time and capital expenditure.

The ASM Pulsar™ ALCVD oxide and metal modules have been described before, as well [3], and also have very similar hardware. The major difference between the high-k reactor and the metal reactor is the use of a uniquely designed solid source delivery system to supply vapor of $ZrCl_4$ and $HfCl_4$ in order to deposit ZrO_2 or HfO_2. H_2O vapor is used as the oxidant. Silicates or aluminates of Zr and Hf are made by using liquid precursors; e.g., $NH_2(CH_2)_3Si(OCH_3)_3$ and TMA, respectively [4]. In the case of metal ALCVD, focus is on TiN [5], TaN, WCN and Ru. All of these layers are made with liquid precursors, like WF_6, $TiCl_4$, NH_3 and $RuCp_2$.

3. Results

Preparation of the Silicon/High-k Interface Layer

SiO_2 and SiON are considered to be ideal candidates to serve as a highly stable and high quality interface layer because of the successful use of these layers as gate dielectric in many generations of CMOS devices. Layer thickness, however, needs to be reduced to values of 0.5nm or below to reach EOT values in the 1nm range. At the same time, the interface layer has to provide a good nucleation surface for the high-k dielectric layer, as well. Fig. 2 provides an example of ellipsometric thickness of thin interface layers as a function of partial pressure of different

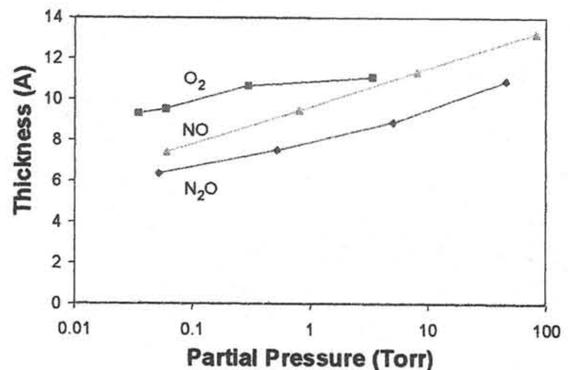

Fig. 2 Thickness of SiO_2 and SiON layers grown in 60 seconds at 800°C at different partial pressures of O_2, N_2O and NO. Thickness measurements are by ellipsometry.

reactive gases. These films are in the right thickness range to be used as interface layers for 1nm EOT gate stacks, keeping in mind that for sub-1nm films, the ellipsometer thickness is up to 0.3nm higher than the corresponding XPS measurement [3].

Deposition of a High-k Layer or Layer Stack

Very promising results have been reported with ALCVD-made unary oxides, like ZrO_2 and particularly HfO_2 [6,7]. On the other hand, (pseudo-)binary oxides, like silicates or aluminates of Hf or Zr, have shown better thermal stability and can remain amorphous under typical CMOS process flow conditions, thus alleviating (perceived?) concerns about grain-boundary leakage paths, dopant diffusion and reliability [8].

Fig. 3 shows new results on an ALCVD-grown, amorphous $Hf_{0.7}Si_{0.3}O_4$ layer after 900°C, 1 sec. N_2 RTA. Typically, leakage current numbers are in the $10^{-4}A/cm^2$ regime for EOT values around 2.0nm.

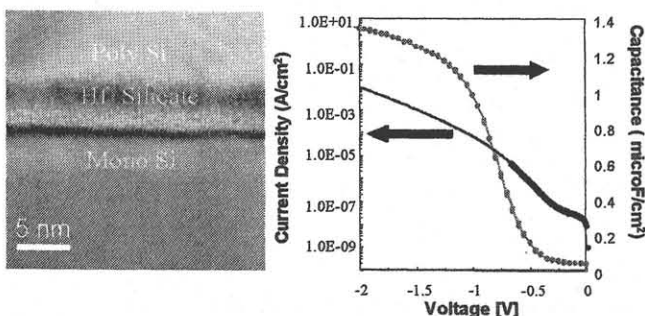

Fig. 3 XTEM (left) and I-V/C-V (right) of a ALCVD $Hf_{0.7}Si_{0.3}O_4$ layer on top of interface oxide after a 900°C, 1 sec. anneal in N_2.

Post-Deposition Processing of the High-k Layer

A post-deposition oxidation in a slightly oxidizing environment may be required to improve the quality of the high-k layer, as well as the SiO_2 interface layer. For that purpose a special, ultra-diluted O_2 environment was established to achieve the goal of improved layer quality while maintaining the EOT value [9]. On top of that, a thin CVD Si_3N_4, or just a nitridation step, may be desired to reduce boron penetration and make the high-k layer more compatible with the subsequent polysilicon CVD process [8]. Thus, the corresponding reactor on the gate stack tool should not only have oxidation and nitridation capabilities but also the capability to deposit thin CVD nitride films.

Deposition of a Polysilicon or Metallic Gate Electrode Layer

Polysilicon is still the default material for use as a gate electrode film on high-k dielectric materials, but poly depletion will result in a considerable contribution to the EOT under device operation conditions. The use of metal or metallic films as a gate electrode eliminates the depletion and boron penetration problems. As a result, it can be concluded that next to a poly Si CVD reactor a metal deposition reactor should also be available for process development. Both reactors are shown in the layout of Fig. 1 where the poly Si CVD process is integrated in the post-deposition (high-k) processing reactor.

In Fig. 4 a cross-section TEM is shown of an ALCVD TiN layer deposited on ALCVD HfO_2. The TiN layer was made by using a $TiCl_4/NH_3$ chemistry [5]. The resistivity of TiN made with this process is in the 200μΩcm range, the Ti/N ratio is very close to 1. The TEM image reveals a high quality interface.

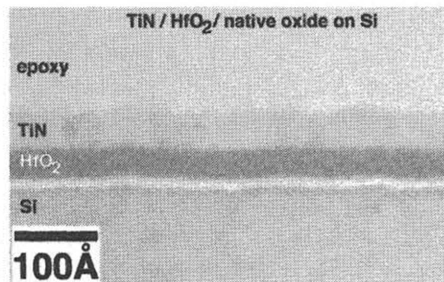

Fig. 4 Cross-section TEM of ALCVD TiN deposited on ALCVD HfO_2.

4. Conclusions

In this paper several critical issues and recent trends in the high-k gate stack formation process were discussed and some recent results were presented. It was shown that the study of high-k gate stack integration issues requires a flexible deposition tool, with process capabilities that include interface layer formation, bulk high-k dielectric deposition, post deposition anneal and polysilicon or metal gate deposition.

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