Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 174-175

B-3-4

Materials and Electrical Characterization of Metal Gate Electrodes on High-k Dielectrics for Advanced CMOS Technologies

Jacob C. Hooker, Robert J.P. Lander, Z.M. Rittersma, Tom Schram[1], Guilherme S. Lujan[1], Jeroen van Zijl[2], Eric van den Heuvel[2] and Fred Roozeboom[2]

Philips Research Leuven
Kapeldreef 75, 3001 Leuven, Belgium
Phone: +32-16-288525 Fax: +32-16-281706 E-mail: jacob.hooker@philips.com
[1]IMEC vzw
Kapeldreef 75, 3001 Leuven, Belgium
[2]Philips Research Labortories Nat.Lab.
Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands

1. Introduction

It is commonly expected that for many CMOS applications, metal gate electrodes and/or high-k dielectrics must be introduced below the sub-100 nm node. A major criterion for metals requires that the work functions match closely those values typically obtained for p^+- (5.2eV) and n^+-type (4.1eV) poly-Si gates after full processing to allow surface channel N- and PMOS transistors with correct V_T's. Furthermore, these metals should be stable with the chosen dielectric.

In order to identify suitable candidates, this work examined possible p^+-type (Mo, MoN) and n^+-type (Ta, TaN) metals on an advanced high-k dielectric stack. Work functions of the metal candidates were extracted before and after a rapid thermal anneal (RTA).

2. Experimental

The metals studied are listed in Table 1 and were capped with 100nm TiN. The optimal high-k stack, Al_2O_3-ZrO_2 -Al_2O_3, was deposited by atomic layer chemical vapor deposition (ALCVD) and was amorphous following deposition (as shown by TEM). The substrates were p-type wafers (5-10 Ω-cm) pretreated with an HF-dip and NH_3 anneal. Plasma etching was used to pattern the capacitor structures. All samples received a forming gas anneal (FGA≡10%H2/N2) at 420°C for 20 min. Some samples received an additional RTA at 1000°C for 10 sec. As a comparison, these metals were also deposited on thermal SiO_2.

Table I Gate stack materials

Metal: t_{phys} = 15 nm	N/Metal Ratio	Deposition Method	High-k Stack: t_{phys} = 3 ,5, 7, 10, 15 nm
Ta	0	RF Sputter	Al_2O_3-ZrO_2-Al_2O_3
TaN	1.05	RF Sputter	Al_2O_3-ZrO_2-Al_2O_3
Mo	0	DC Sputter	Al_2O_3-ZrO_2-Al_2O_3
MoN	1	DC Sputter	Al_2O_3-ZrO_2-Al_2O_3

Capacitors of area $6.4\times10^{-5}cm^2$ were used for high-frequency (HF) CV measurements. The NCSU program [1] was used to extract the equivalent oxide thickness (EOT) and flat-band voltage (V_{FB}). TEM, XRD, and RBS were used for materials characterization. Resistivity measurements (Table II) were made using the 4-point probe method.

Table II Resistivity, R_{sp} (mΩ-cm), of the various metals

Metal	As Depo.	FGA 420°C, 20 min	RTA 1000°C, 10 sec
Ta	0.229 ± 11%	0.112 ± 5%	0.392 ± 50%
TaN	0.310 ± 10%	0.355 ± 5%	0.530 ± 5%
Mo	0.015 ± 7%	0.011 ± 5%	0.013 ± 5%
MoN	0.439 ± 10%	0.383 ± 5%	0.157 ± 5%

3. Results and Discussion

In Fig.1 are plotted typical HF-CV measurements with a Ta gate electrode and various dielectric thicknesses.

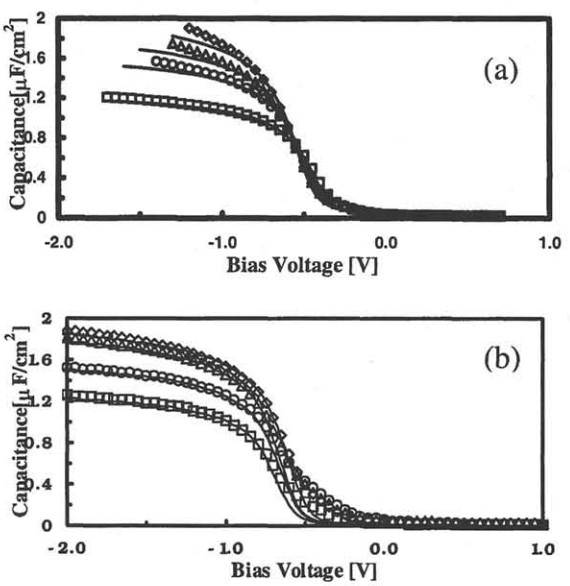

Fig. 1 HF-CV measurements of (□)15, (○)10 (Δ)7 and (◊)5 nm Ta on optimal high-k stack: (a)420°C FGA for 20 min and (b) 1000°C RTA for 10 sec. Solid lines are theoretical fits.

Plots of EOT vs. V_{FB} were used to determine the metal work function, ϕ_M, with the aid of the following equation,

$$\phi_m = \phi_{Si} + V_{FB} - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

where C_{ox} is the oxide capacitance and ϕ_{Si} is the work function of the Si substrate. The fixed charge, Q_{ox}, is assumed independent of the oxide thickness. This was done for each of the metals after both an FGA at 420°C for 20 min and after an RTA at 1000°C for 10 sec. The results are plotted in Fig. 2.

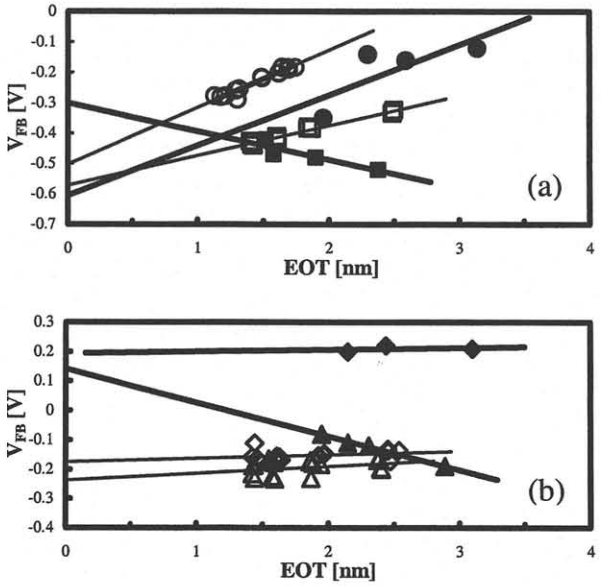

Fig. 2 V_{FB} as a function of EOT for (a) (□)Ta and (○)TaN; (b) (Δ)Mo and (◊)MoN after FGA at 420°C, 20 min. Filled symbols correspond to RTA at 1000°C for 10 sec.

The calculated work functions are summarized in Table III. Also listed for comparison are the values determined on thermal SiO_2. Within experimental error, the values on high-k and SiO_2 are very similar suggesting the metal work functions are independent of these dielectrics. This is in contrast to what has been reported previously [2], although this study does not completely disprove the latter.

These results show that TaN and MoN are promising metals for gate electrodes in NMOS and PMOS devices, respectively, even after thermal processing. However, a non-negligible change in the work functions of the metal/high-k stacks (except for TaN) occurs after the RTA at 1000°C for 10 sec. XRD measurements and high-resolution XTEM (Fig. 3) suggest that the bulk metal and interface properties are quite stable. Further proof of the metal stability is shown in the similar work function values of the Mo/SiO_2 stack before and after an RTA. Thus, it may be possible to attribute some of these changes in electrical behavior to partial crystallization of the high-k stack as has been reported in other studies [3]. Furthermore, it has been observed that crystallization of these materials can be influenced by factors such as the film thickness and the materials with which it is in contact. For most of the metals, this resulted in an increase of 0.3 eV.

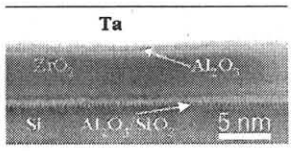

Fig. 3 TEM image of Ta/high-k stack; 1000°C RTA for 60 sec. Top Al_2O_3 layer is appr. 0.5 nm. Bottom 1nm layer is a mixture of Al_2O_3 and SiO_2. Dark contrast at the Si/oxide interface is due to the NH_3 surface treatment that strains the Si lattice.

Table III Metal Work Functions in eV

Metal	Dielectric	FGA 420°C, 20 min.	RTA 1000°C, 10 sec.
Ta	Al_2O_3-ZrO_2-Al_2O_3	4.3 ± 0.1	4.6 ± 0.1
TaN	Al_2O_3-ZrO_2-Al_2O_3	4.4 ± 0.1	4.3 ± 0.1
Mo	Al_2O_3-ZrO_2-Al_2O_3	4.7 ± 0.1	5.0 ± 0.1
MoN	Al_2O_3-ZrO_2-Al_2O_3	4.8 ± 0.1	5.1 ± 0.1
Ta	SiO_2	4.3 ± 0.1	Reaction
TaN	SiO_2	4.3 ± 0.1	Reaction
Mo	SiO_2	4.9 ± 0.1	5.0 ± 0.1*
MoN	SiO_2	4.9 ± 0.2	No results

*RTA at 800°C for 30 sec

4. Conclusions

It has been shown that Mo and MoN are suitable metal gate candidates for PMOS Devices after an RTA at 1000°C for 10 sec. TaN is also promising for NMOS. Although favorable values of the work functions were determined for most of the metals under various annealing conditions, the high-k stack used in this study is unlikely to be viable due to crystallization and the abundant presence of charge defects. However, by introducing a metal oxide with a stronger affinity for oxygen, e.g. HfO_2, and better thermal properties, it will be possible to improve the properties of gates stacks for advanced CMOS technologies using these metal candidates.

Acknowledgments

Thanks to Philips CFT for providing the materials analysis and Dr. B. Pawlak for some of the R_{sp} measurements.

References

[1] J.R. Hauser and K. Ahmed: *Conference on Characterization and Metrology for ULSI Technology 1998*, (1998) p.235.

[2] Y.-C. Yeo, R. Pushkar, Q. Lu, R. Lin, T.-J. King and C. Hu: Symp. VLSI Technology, 2002, p. 49.

[3] G.D. Wilk, R.M. Wallace, and J.M. Anthony: J. Appl. Phys. **89**, 5243 (2001); references therein.