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Novel Binary Alloy Gate Electrodes for Metal Gate MOS Devices

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Abstract

This paper explores the characteristics of the binary alloys Pt-Ta and Ti-Ta for gate electrode application, and demonstrates that the alloys are superior to pure metals in many aspects. The alloys have better thermal stability and better adhesion with dielectric and inner chemical activity. What's more, with a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16eV to 5.0eV continuously, thereby making them suitable for use in all device applications.

1. Introduction

As conventional CMOS devices are scaled down to improve performance, gate engineering becomes a crucial issue. It is believed that using a metal gate instead of a poly-Si gate can completely solve the gate depletion and boron penetration problems. Using a metal gate can also allow for a reduced process temperature. But not all metals are applicable; a metal gate must have different work functions (Φ_m) for different device applications.

However, work function modulation technology of the metal gate has not been well established. It was reported that the Φ_m of metal nitrides could be modulated by varying the nitrogen content [1-3]. Unfortunately, the magnitude of modulation is not large enough. Recently, metal alloys were proposed to solve the problem of work function incompatibility [4,5]. This study uses novel binary alloy systems (Ta-Pt and Ta-Ti) to modulate Φ_m. We found that the Φ_m can be modulated from 4.16eV to 5.0eV, continuously. Furthermore, our proposed alloys have good thermal stability and inert chemical activity. All these characteristics of our proposed alloys make them very promising candidates as gate electrodes.

2. Experiments

A simple MOS capacitor structure was fabricated to characterize the binary alloy systems. The process flow is listed in Table-1. Ta_xPt_y and Ta_xTi_y films were co-sputtered on thermally grown SiO_2, with various sputtering powers from 30W to 150W. Table-2 lists the deposition conditions. The gate electrodes were patterned using the lift-off process. After gate patterning, samples were annealed in N_2 ambient at 400, 500, and 600℃ for 30 min. The Φ_m of 400℃ annealed samples was extracted by comparing the measured C-V curves with the theoretical C-V curve, assuming oxide charges are negligible. Interface state density (D_{it}) at the SiO_2/Si interface, and electron tunneling barrier height (Φ_B) at the alloy/SiO_2 interface, were also extracted.

3. Results and Discussion

The atomic compositions of alloys were analyzed with Rutherford Back Scattering spectroscopy (RBS) and are listed in Table-3. Fig. 1 shows the C-V curves of all samples. The C-V curve of the n+ poly-Si gate MOS capacitor is also shown. With increasing contents of high Φ_m elements (Ta or Pt), the C-V curve shifts toward the right. Fig.2 shows the extracted Φ_m of 400℃ annealed samples. The $Ta_{0.63}Ti_{0.37}$ alloy shows Φ_m of about 4.16eV, which is close to the Φ_m of n+ poly-Si, and is suitable for NMOSFETs. On the other hand, the $Ta_{0.58}Pt_{0.42}$ alloy exhibits high Φ_m of about 5.0eV, which is suitable for PMOSFETs. The most important observation is that the Φ_m can be modulated continuously by adjusting the atomic composition of the alloy. This property allows for the use of the alloy system for the gate electrode in any application. For example, fully-deplete SOI devices require Φ_m of 4.6 eV, and can be achieved using the $Ta_{0.74}Pt_{0.26}$ alloy.

Figs. 3 and 4 show the sheet resistances and the changes of equivalent oxide thickness (EOT) of alloys after annealing at various temperatures, respectively. No sheet resistance degradation is observed with the increase of annealing temperature. The change of EOT is less than 1.5%, implying the increase of oxide thickness is less than 0.15nm. Figs. 5(a) and 5(b) show the X-Ray Diffraction (XRD) spectrums of $Ta_{0.58}Pt_{0.42}$ and $Ta_{0.63}Ti_{0.37}$, respectively. The diffraction spectrums of alloys annealed at different temperatures are almost identical. The absence of interfacial interaction between the alloys and the SiO_2 is shown in Fig. 6. All of these results confirm the thermal and chemical stability of the gate structure.

Fig. 7 shows that the corrected V_{fb} decreases with the increase of annealing temperatures. This is due to the increase of D_{it} and the drop of Φ_B (See Figs. 8 and 9), which may be caused by the non-optimized oxidation process. A stable V_{fb} could be expected with thinner EOT and optimized gate dielectric formation process.

4. Conclusion

We have demonstrated a novel work function modulation scheme with binary alloy systems (Ta-Pt and Ta-Ti). The work function of alloys can be controlled to satisfy the threshold voltage of either bulk or SOI CMOS devices. Together with good thermal stability and inert chemical activity, the proposed alloys are very promising candidates as gate electrodes.

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References

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- N-type Si(100) substrate
- RCA clean
- SiO_2 growth (11nm)
- Alloy deposition with various power
- Electrode patterning with lift-off process
- Annealing in N_2 ambient at various temperatures
- Backside metallization with Al

Table.1 Fabrication process of MOS capacitor.

	PVD Power		
Sample ID	Ta	Pt	Ti
A1	50W	0W	50W
A2	150W	0W	0W
A3	100W	30W	0W
A4	50W	30W	0W
A5	30W	30W	0W
A6	0W	30W	0W

Table.2 Deposition conditions of alloys.

	Composition (%)		
Sample ID	Ta	Pt	Ti
A1	63	0	37
A2	100	0	0
A3	74	26	0
A4	65	35	0
A5	58	42	0
A6	0	100	0

Table.3 Atomic composition identified with RBS analysis.

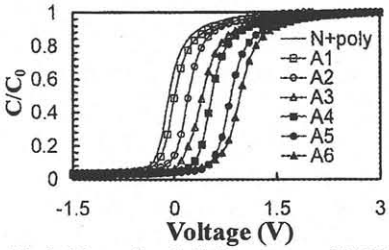


Fig.1 Normalized C-V curves of MOS capacitors with various gate materials after annealing in N2 ambient for 30 min at 400℃.

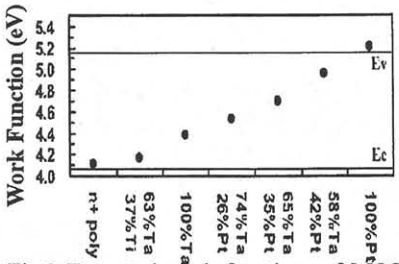


Fig.2 Extracted work functions of MOS capacitors with various gate materials after annealing in N2 ambient for 30 min at 400℃.

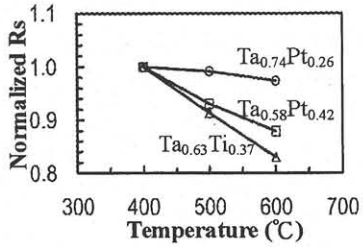


Fig.3 Normalized sheet resistance versus annealing temperature of samples A1, A3, and A5.

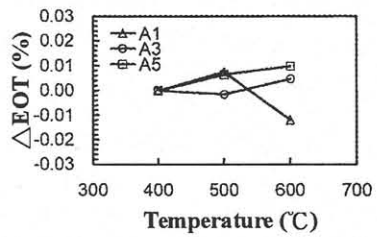
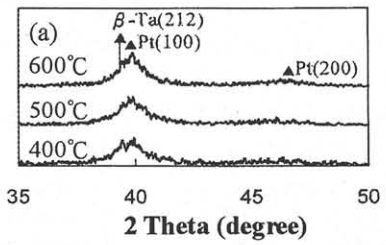


Fig.4 Change of EOT versus annealing temperature of samples A1, A3, and A5.



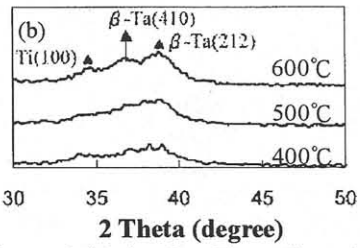


Fig.5 XRD spectrums of (a) the $Ta_{0.52}Pt_{0.48}$ alloy and (b) the $Ta_{0.63}Ti_{0.37}$ alloy after annealing at various temperatures.

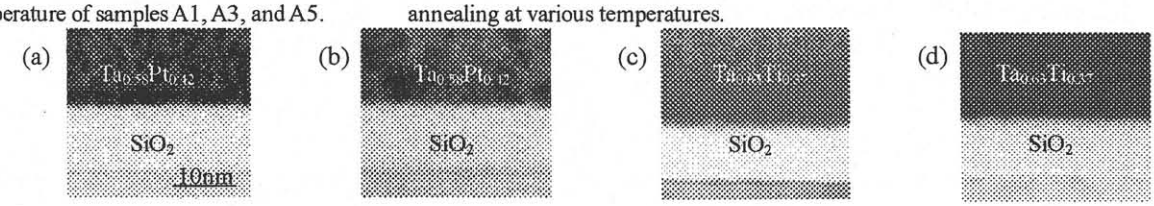


Fig.6 TEM photographs of (a) the 400 ℃ annealed $Ta_{0.52}Pt_{0.48}$ alloy, (b) the 600 ℃ annealed $Ta_{0.52}Pt_{0.48}$ alloy, (c) the 400 ℃ annealed $Ta_{0.63}Ti_{0.37}$ alloy, and (d) the 600 ℃ annealed $Ta_{0.63}Ti_{0.37}$ alloy.

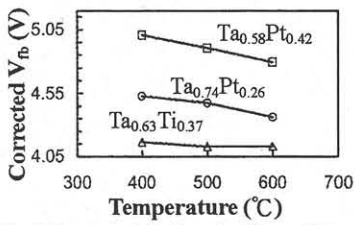


Fig.7 Corrected flat-band voltage (V_{fb}= Φ_m-Q_{eff}/C_{ox}) versus annealing temperatures.

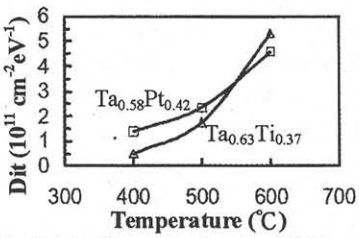


Fig.8 Interface state density (Dit) versus annealing temperatures extrapolated from high-low frequency C-V measurement.

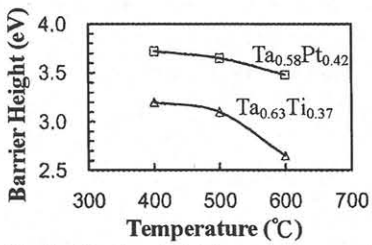


Fig.9 Barrier height versus annealing temperatures extrapolated from Fowler-Nordheim analysis.