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Negative-Bias-Temperature Instability in Ultra Thin Nitride/Oxide Stack Gate Dielectric

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1.Introduction

Negative-bias-temperature instability (NBTI) represents one of the major reliability concerns for deep sub-micron PMOS transistors [1] ~ [4]. Recently, it was shown that nitride/oxide (N/O) stack is a potential candidate for replacing thermal oxide as the gate dielectric in sub-100 nm nodes [5]. In this work, we investigate and evaluate the NBTI of the devices with N/O gate stack.

2.Experimental

Dual-gate p- and n-channel MOSFETs were fabricated using standard CMOS twin-well technology. Nitride/oxide (N/O) stack or thermal oxide was used as gate dielectric. The N/O stack consists of 0.8-nm bottom oxide and 1.4-nm high-quality nitride. The bottom oxide was grown by wet oxidation in a catalysis oxidation chamber. Prior to CVD nitride deposition step, a remote plasma nitridation (RPN) treatment was performed by exposing the bottom oxide to a high-density remote helicon-based nitrogen discharge at 450 ℃ for 30 s. This RPN treatment provides a thin oxynitride layer of smooth and high nitrogen concentration on the oxide top surface, and serves to buffer the structural mismatch between the bottom oxide and the nitride film [6]. A post-deposition annealing was performed in N_2 ambient to eliminate structure defects. For splits with thermal oxide gate dielectric, the oxide was thermally grown by wet oxidation, followed by a RTA treatment in NO ambient. Equivalent oxide thickness (EOT) for both splits is determined to be about 1.6nm, using a CV method that takes into account both the quantum mechanism and the poly gate depletion effect.

To evaluate device degradations due to bias-temperature stress (BTS), the devices were subjected to stress configuration shown in Fig.1 with negative gate-bias (– 1 V ~ –2.3 V) and at elevated temperature (150℃). During the stressing, drain/source and substrate were all grounded. Device parameters including threshold voltage (Vth), subthreshold swing, and gate leakage current, were measured using an HP4156A parameter analyzer before and after the BT stressing.

3.Results and Discussion

Figure 2 shows carrier separation results for devices with N/O stack dielectric. As pointed out previously [2], Ig is dominated by valence-band holes tunneling from the inversion layer in the low voltage regime. When $|Vg|$ is high enough (e.g., > 2.4 V in Fig, 2), Ig becomes dominated by valence-band electrons tunneling from p+ gate electrode.

Figure 3 shows the Vth shift as a function of stress time for oxide and N/O samples. The shift is larger for N/O devices under a fixed Vg condition. It is also found that, the exponent value for the N/O sample at Vg=-2V (~0.2) is much smaller than that of the oxide counterpart, as well as the N/O sample at Vg = -1V (~0.28). This indicates that the degradation mechanism could be quite different for the N/O gate stack under high gate-bias condition.

Figure 4 depicts the NBTI lifetime as a function of stress voltage. Criterion for determining lifetime is the time that Vth shift reaches 30 mV. The lifetime for N/O samples will be much shorter than that of the oxide ones if a linear extrapolation based on fitting the data points in the high Vg regime (>-1.8V) is used. Fortunately, the practical data for the N/O samples at a low Vg of -1 V are much longer than the prediction, as shown in Fig. 4.

In order to understand the effects in more detail, we measured and compared the subthreshold characteristics of the samples both immediately and 42 hours after the BTS. The results are shown in Fig. 5. Vg of –2V was used. In Fig. 5a, it is clearly seen that Id-Vg characteristics of N/O devices almost recover to pre-stress value after 42 hours. In contrast, no noticeable recovery is observed for the devices with oxide gate dielectric.

The aforementioned results imply that significant amount of holes may be trapped in the N/O gate dielectrics during the BTS. In line with this, we propose the band diagrams shown in Fig. 6 to explain the NBTI degradation and recovery behaviors for the N/O gate dielectric. In Fig. 6a, valence-band holes tunneling from the substrate during the BTS are trapped in the nitride layer. After the BTS, the trapped holes gradually return to the substrate (Fig. 6b), so the device subthreshold characteristics recover.

4.Conclusions

NBTI of deep sub-micron p-channel MOSFETs with N/O gate stack was explored in this work. Our results show that trapped holes in N/O gate dielectric as a result of BTS cause aggravated NBTI. Moreover, linear extrapolation of device lifetime from the high Vg regime tends to greatly underestimate the device lifetime at low Vg.

Acknowledgment

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References

[1] C. E. Blat *et al.*, J. Appl. Phys. **69**, p.1712 (1991).
[2] N. Kimizuka *et al.*, Symp on VLSI Technology, (1999) p.73.
[3] R. Thewes *et al.*, Tech. Dig. of IEDM, (1999) p.81.
[4] N. Kimizuka *et al.*, Symp. on VLSI Technology, (2000) p.92.
[5] B. Yu et al., Symp. on VLSI Technology, (2001), p.9.
[6] S. F. Ting *et al.*, IEEE EDL, **22**, p.327 (2001).

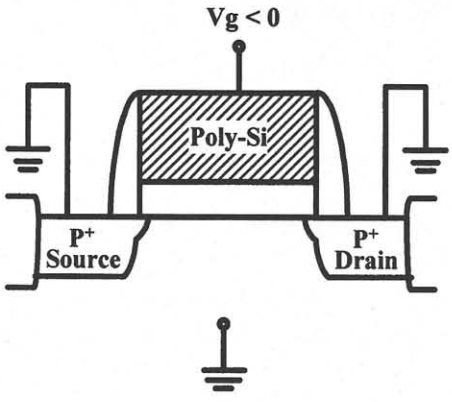


Fig. 1. Configuration for NBTI stressing.

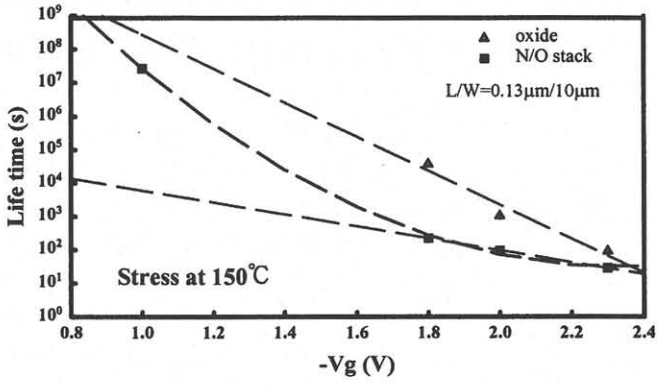


Fig.4. Device lifetime vs. stress voltage for different gate dielectric materials.

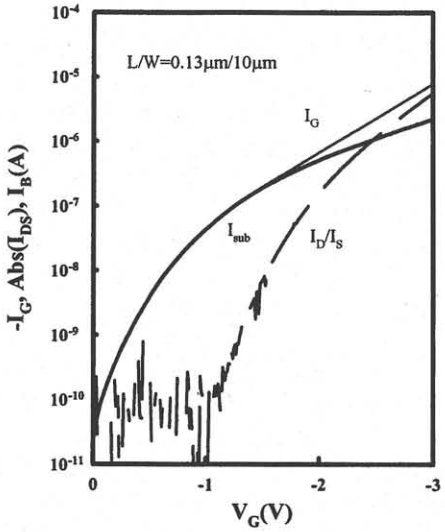


Fig. 2. Carrier separation results for pMOSFET with EOT=1.6nm thick gate oxide, which is similar to N/O stack gate.

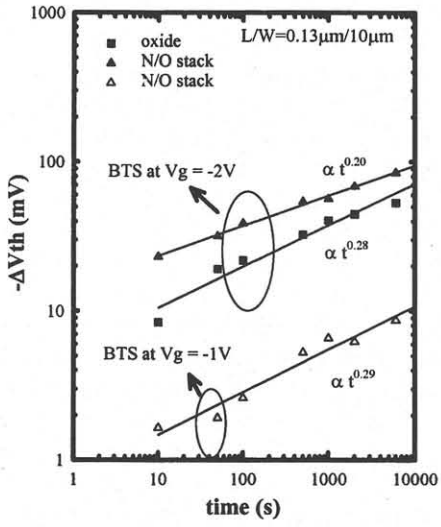
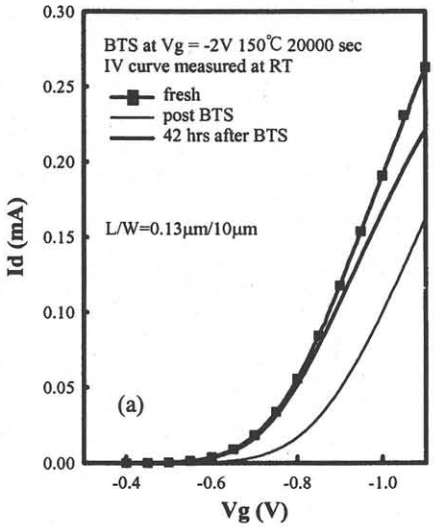


Fig.3. Vth shift vs. stress time for N/O stack and thermal oxide.



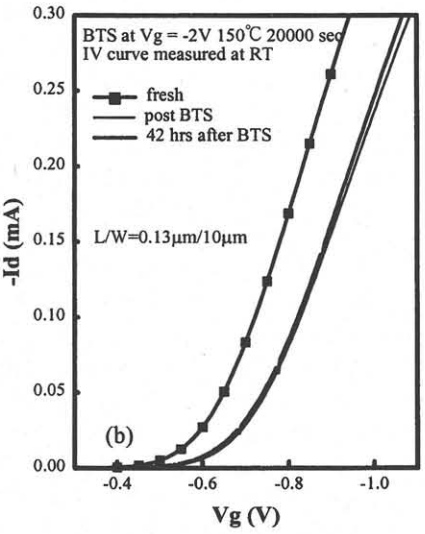


Fig.5. Id-Vg characteristics for pMOSFETs measured before, immediately after, and 42 hrs after BTS at –2V for (a) N/O stack, and (b) thermal oxide.

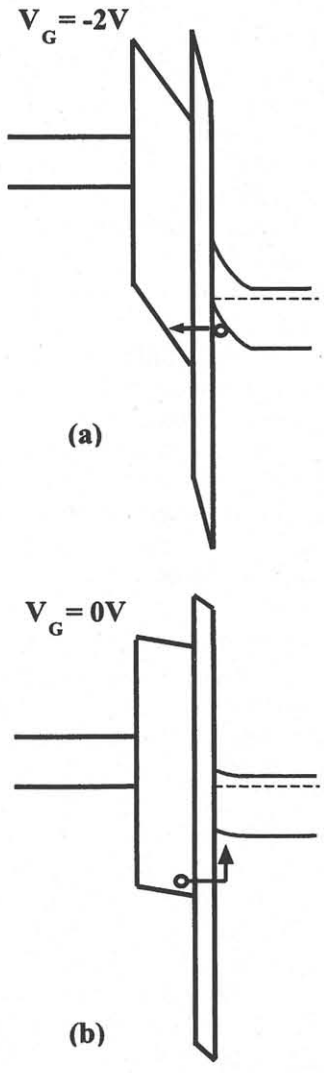


Fig. 6. N/O stack gate energy diagrams for (a) BTS at Vg = –1V, and (b) Vg = 0 V.