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A New Plasma Dry Cleaning Method Applied to Contact and Gate Pre Cleaning.

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1. Introduction

High-density DRAMs require very small and deep contact holes. Moreover, Inter Layer Dielectric (ILD) is mostly a multi layer composed of various kinds of oxide films. Thus it's difficult to clean the bottom of the hole by conventional HF based solution without hole enlargement and difference of etching rate among oxides. High performance CMOS Logic devices require very thin gate oxide. This requirement becomes even more severe for high-k gate dielectrics because extremely thin interfacial oxide(oxinitride) layer(0.5~0.7nm) is required. So there is a strong need for native oxide removal process which can be clustered together with gate dielectrics formation chamber.

A powerful solution to these problems is dry cleaning process. Several NF_3 based dry cleaning processes have been studied [1][2]. We developed advanced wafer surface cleaning technology with NF_3 assisted with H_2/N_2 downflow plasma. The most outstanding feature of this technique is the self-limiting etching phenomena which enables free-of-selectivity etching to the various kinds of oxide films. Therefore, contacts can be cleaned with minimum enlargement of holes, Moreover, this process has a potential to be used for gate pre-cleaning as a cluster tool.

2.Experiment

Fig.1 is chamber schematic. Hydrogen and Nitrogen gases are injected into the quartz tube as shown in Fig.1. These gases are discharged with microwave power which is introduced with plasma applicator. NF_3 gas is introduced through direct inlets into the reaction chamber which is not plasma excited to avoid decomposition of NF_3 which generates F-radicals and Si etch occurs. The main process has two steps. The first step is generating etching species with downflow plasma and NF_3 to react with native oxide(Downflow Step). The second step is heating up the wafer to evaporate the byproduct on the wafer surface and obtain clean surface(Annealing Step).

FT-IR spectra measurement was carried out on treated surface. To estimate etching thickness, thermal oxide film was measured by ellipsometry. To evaluate the process performance, contact array TEG was used for contact resistance measurements and MOS capacitor was fabricated for gate oxide characterization respectively. C-V, I-V measurements were carried out by Agilent 4071 parametric test system.

3.Results and Discussion

Fig.2 shows the change of IR spectra for each dry cleaning process steps. 8inch Si substrate with 3nm thermally grown oxide was used for the sample. By Downflow step, IR signal corresponding to SiO_2 bond decreased while the signal corresponding to Si-F and N-H increased, showing that SiO_2 reacts with activated NF_3 and were converted into Si-F and N-H. After Annealing step the signal for Si-F and N-H disappeared, showing that S-F and N-H based by-products were evaporated during Annealing step. The signal for SiO_2 is not changed, showing that Si-O bond was already completely removed at the Downflow step.

Fig.3 and Fig.4 show etching thickness of thermal oxide depending on the first step (downflow) time and wafer stage temperature respectively. Etching thickness increased with process time and became saturated. This saturation behavior is the consequence of pile-up of byproduct which acts as a barrier for further reaction. The incubation time was not observed. Moreover etching thickness decreased drastically at higher temperature than 20deg.C. So etching reaction rate is thought to be related with adsorption of etching species on SiO_2 surface considerably.

Fig.5 shows TDS spectra of dry cleaned Si surface. Observed double peaks suggest that the surface is basically hydrogen terminated.

Fig.6 shows the SEM images of contact holes with stacked ILD materials. The sample(a) processed with 0.5%DHF for 1min and sample(b) was exposed to the dry cleaning for 60min. The step-shape due to the etching rate difference was observed on the DHF cleaned sample. However no step was observed on the sample with downflow plasma cleaning even processed for 60 minutes.

Fig.7 shows the resistance of $n+$ poly-Si/Si contact. The contact resistance of the sample with downflow plasma treatment was almost the same as that of DHF treatment, and even lower for the smallest hole size, The result that the interface at poly-Si and Si-substrate is well controlled with the downflow plasma cleaning.

Fig.8 shows C-V curves of 1.5nm thermal oxide with different gate preclean processes, measured by two frequencies C-V method. C-V curve is precisely the same for this pre-clean and DHF-last, showing both electrical thickness and interface properties are the same.

Furthermore, gate leakage current (J_g) at V_{fb}-0.4v is shown in Fig.9. All J_g-Tox plots were on a line. Therefore, gate leakage current on this cleaned surface was as same as that on DHF cleaned surface.

4. Conclusions

We demonstrated $H_2/N_2/NF_3$ based remote plasma assisted dry cleaning process for native oxide removal prior to contact filling or gate oxidation.

Selectivity-free contact pre-clean was achieved by down flow plasma process, and the contact resistance is as low as that of wet pre-cleaning.

The C-V characteristics of gate oxide on dry cleaned Si surface was quite as same as those on conventional DHF cleaned surface, thus suggesting the potential use for gate pre-cleaning.

References

[1] Y.Horiike, K.Kawamura Japan.Patent JPH4-98895

[2] J.Kikuchi et. al. Dry Proc. Symp.(1993) 14 Y. Aoyagi and Y. Miyamoto, Jpn. J. Appl. Phys. **43**, 278 (1998)

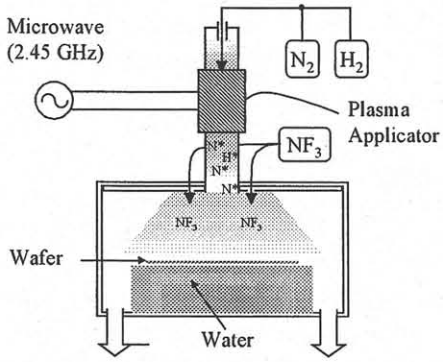


Fig.1 Schematic of Dry Cleaning Chamber.

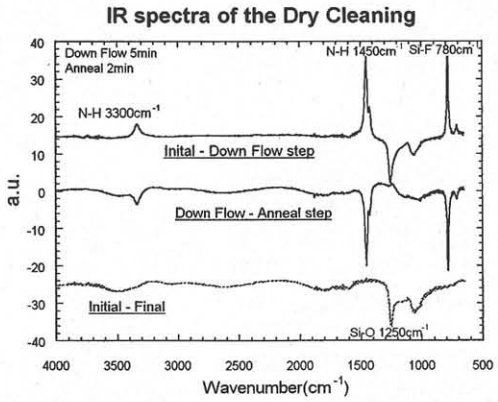


Fig.2 FTIR-ATR spectra of dry cleaned surface.

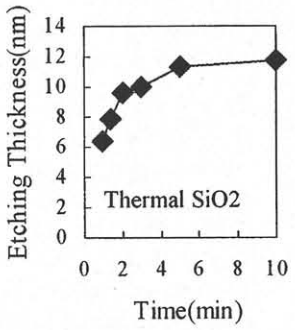


Fig3. Etching thickness vs. downflow time.

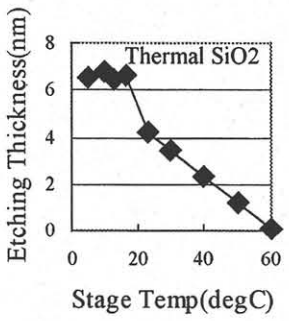


Fig.4 Etching thickness vs. wafer stage temperature.

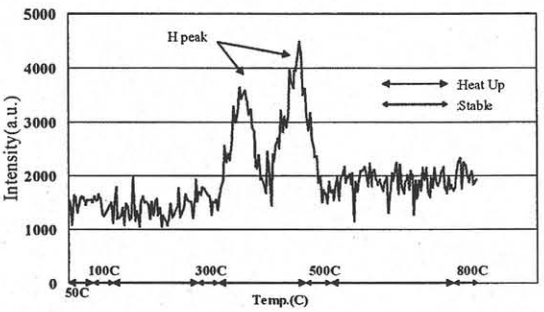
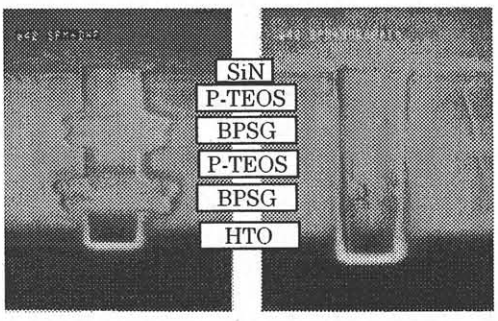


Fig.5 Hydrogen peaks by TDS on dry cleaned Si surface.



(a)0.5% DHF 1min (b)Dry Cleaning 60min

Fig.6 SEM photographs of contact hole

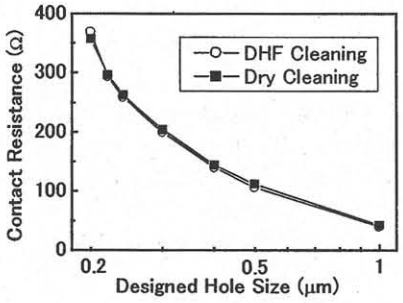


Fig.7 Contact resistance for various cleaning. Hole depth is 1.0μm.

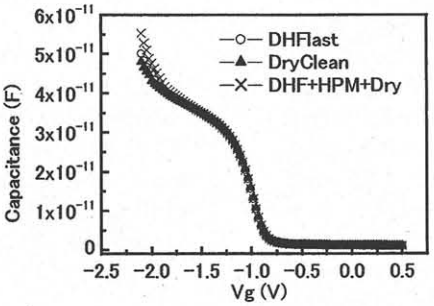


Fig.8 Two frequencies C-V curves. Tox=1.5nm, Gate area=2500μm^2

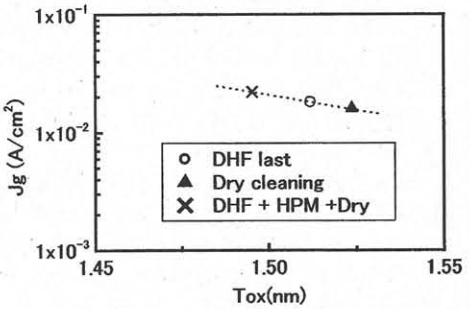


Fig.9 Gate Leakage Current.