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Electrical Characterization of Aluminum-Oxynitride Stacked Gate Dielectrics Prepared by a Layer-by-Layer Process of Chemical Vapor Deposition and Rapid Thermal Nitridation

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1. Introduction

Aluminum oxide based dielectrics have been extensively studied as a promising alternate to conventional SiO_2–based gate dielectrics [1–3] because of their high thermal stability against crystallization compared with other candidates such as ZrO_2 and HfO_2. For the uniform growth of Al_2O_3 films with precise thickness control and without damages inherent in a sputtering method, an atomic layer (AL–) CVD technique [4, 5], in which generally $Al(CH_3)_3$ and H_2O alternately react with the growth surface at a temperature as low as 300°C, respectively, has been developed so far. However, incompleteness at each step in AL–CVD, if any, results in the formation of a loose film network with undesirable carbon incorporation. In fact, significant dopant diffusion through CVD–Al_2O_3 to the Si(100) substrate was reported [2, 6]. We have developed a new deposition method for Al oxynitrides (AlO_x:N), where the LPCVD from a gas mixture of N_2O + AlH_3 stabilized with an alkylamine and subsequent NH_3 annealing are alternately repeated, and applied to the formation of a AlO_x:N/SiN_x stacked gate dielectric structure [7].

In this paper, we report electrical properties and the reliability of the AlO_x:N/SiN_x stacked dielectrics in n^+–poly Si gate MIS capacitors.

2. Experimental

MIS capacitors with phosphorous doped n^+–poly Si gates were fabricated on p–type Si(100) wafers with LOCOS patterned structures. Si wafers were cleaned by an NH_4OH:H_2O_2:H_2O=0.15:3:7 solution at 80°C for 10min. Then, the surfaces were terminated with hydrogen in a 0.1%HF+1%H_2O_2 solution to minimize the surface microroughness. Before AlO_x:N film growth, the wafer was heated up to 700°C in ambient NH_3 at 5Torr by IR radiation for the surface nitridation to stabilize the surface against oxidation. Subsequently, AlO_x:N films were formed on such nitrided Si(100) surfaces by alternately repeating the sub–nanometer deposition of Al_2O_3 from a N_2O+AlH_3:$N(CH_3)_2C_2H_5$ gas mixture at 300°C under 0.6Torr and the rapid thermal nitridation in ambient NH_3 of 5Torr at 700°C in a layer–by–layer fashion. To remove bonded hydrogen and to make up for the oxygen deficiency, 700°C anneal was preformed in ambient O_2 at 100Torr after the layer-by-layer film growth. Very uniform film formation was confirmed by AFM observations. Also, cross-sectional TEM images confirmed the smooth and flat interface. From the angle-resolved XPS analysis, we found that ~1.0nm–thick SiN_x layer was formed at the interface and the mean nitrogen concentration in the AlO_x:N films so prepared was increased from 4 to 21at.% as the film thickness, corresponding the number of the niridation step, increased from 3.3 to 10nm.

3. Results and Discussion

The capacitance–voltage (C-V) characteristics of n^+poly-Si/AlO_x:N/SiN_x/Si(100) capacitors are shown in Fig. 1, which were derived from raw C–V curves measured at 400 and 800kHz to eliminate the influence of leakage current on the impedance measurement. For all the cases, a similar hysteresis due to the electron injection into oxide traps is observable with a width ranging from 60 to 160mV. The flat–band voltage shifts toward the positive gate voltage side with increasing capacitance equivalent thickness (CET) of the stacked dielectric determined from the maximum capacitance value, indicating the negative fixed charges as in the case of Al_2O_3 [1]. As represented in Fig. 2, the negative net charge per unit area is almost constant at $3.9\times10^{12}cm^{-2}$ independent of the film thickness. Considering the fact that generally there exist positive fix charges in silicon nitride, the result of Fig. 2 suggests a negative charge profile decaying as a function of a reciprocal distance from the poly–Si/AlO_x:N interface. From the relationship between the physical thickness and the CET, the dielectric constant of the AlO_x:N/SiN_x stacked dielectric is 8.9, being almost identical to the reported value for Al_2O_3 [5, 8]. Also, the leakage current density through the AlO_x:N/SiN_x stacked dielectrics is almost the same level as reported in Al_2O_3 and is suppressed markedly from the direct tunnel current through SiO_2 with the same CET (Fig. 3). A weak temperature dependence of the leakage current as seen in Fig. 4 implies that the leakage current due to electron tunneling is predominant. An increase in the current level with temperature observed in the dielectric voltage range of 0.6–2V might be attributable to the electron tunneling through shallow defects existing near the poly–Si/AlO_x:N interface. The hard breakdown (HBD) voltage measured at a ramp–up rate of 60mV/s for 100 capacitors is almost constant and one can determine the breakdown filed of the AlO_x:N/SiN_x stacked dielectrics to be ~8MV/cm in consistence with the general correlation between the breakdown field and the dielectric constant for various dielectrics as shown in Fig. 6. Figure 7 represents the time-dependent dielectric degradation measured under constant current stress at 200A/cm^2. Two distinct degradation modes were observed, being quite similar to stress–induced leakage current (SILC) and soft breakdown (SBD) observed in dielectric degradation of ultrathin SiO_2. As seen in Fig. 8, the flat–band voltage shift is decreased with increasing stressing time, implying the annihilation or compensation of negative fixed charges by structural changes in the staked dielectrics whose mechanism is not clear yet. The Weibull slope β for time–to– SBD and HBD evaluated as a function of the physical thickness are summarized in Fig. 9 in comparison with the results reported for pure Al_2O_3 and SiO_2. No significant difference in the β value between thick AL–CVD Al_2O_3 and the AlO_x:N/SiN_x stacked dielectrics is observed. Note that, for cases thinner than 6nm, the β value of the stacked dielectrics is almost the same as that of SiO_2.

4. Conclusions

The AlO_x:N/SiN_x stacked gate dielectrics have shown that negative fixed charges characteristic of almina are as high as $3.9\times10^{12}cm^{-2}$ in the effective net charge density and the effective dielectric constant and breakdown field are 8.9 and 8MV/cm, respectively as in the case of Al_2O_3. The dielectric degradation process similar to the transition from SILC to SBD reported in SiO_2 and a fairly good reliability comparable to

thermally–grown ultrathin SiO_2 have been demonstrated for the stacked gate dielectrics.

5. Acknowledgements

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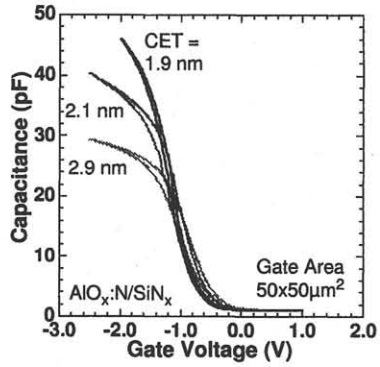

Fig. 1: Capacitance–voltage characteristics for n^+poly–Si gate capacitors with AlO_x:N/SiN_x stacked dielectrics.

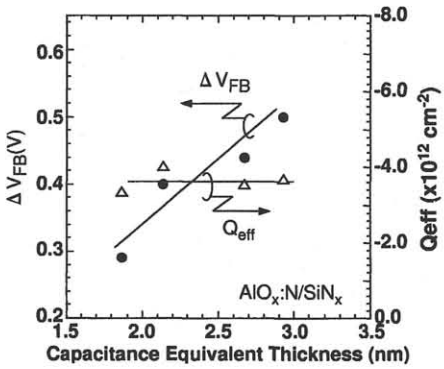

Fig. 2: Capacitance equivalent thickness (CET) dependence of the flat–band voltage shift ΔV_{FB} and effective net negative charge density Q_{eff}.

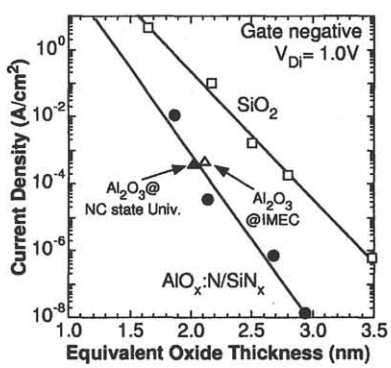

Fig. 3: Current density through the AlO_x:N/SiN_x stacked dielectiric at a dielectric voltage of 1.0V as a function of the equivalent thickness. The reported data for Al_2O_3 [5, 8] and SiO_2 [9] also shown as references.

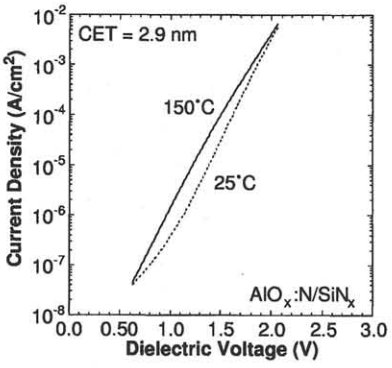

Fig. 4: Current–voltage characteristics for the AlO_x:N/SiN_x stacked dielectiric with a CET of 2.9nm measured at 25 and 150°C.

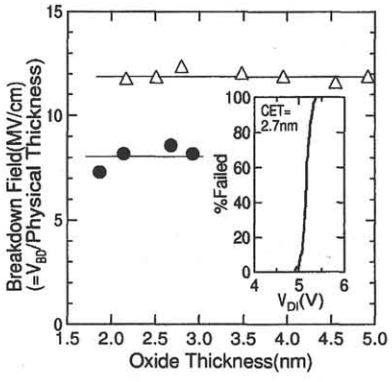

Fig. 5: Hard breakdown fields determined for the AlO_x:N/SiN_x stacked dielectirics and thermally–grown SiO_2 layers. The inset shows the cumulative failure rate for the stacked dielectrics with CET=2.7nm.

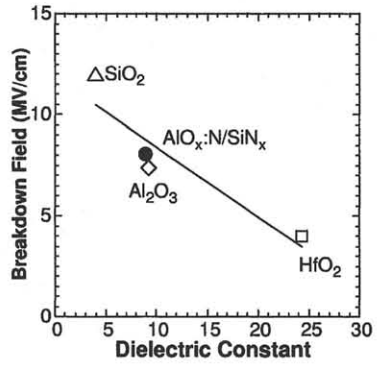

Fig. 6: Relationship between the breakdown field and the dielectric constant for different dielectric materials.

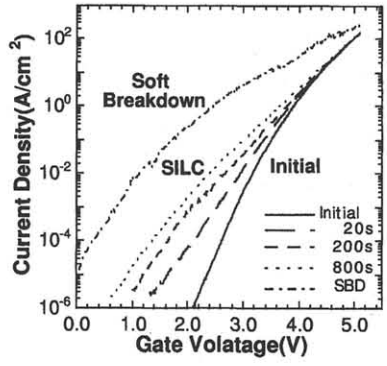

Fig. 7: I–V characteristics before and after constant current stress at 200A/cm^2.

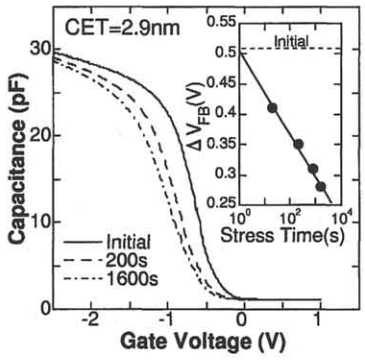

Fig. 8: C–V characteristics for the stacked dielectrics with CET=2.9nm before and after constant voltage stress at a gate voltage of −4.5V. The inset shows the temporal change in ΔV_{FB} under the constant voltage stress.

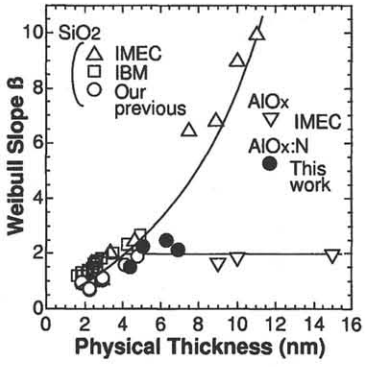

Fig. 9: Physical thickness dependences of the Weibull slope β for the stacked dielectrics, SiO_2 [5, 10, 11] and Al_2O_3 [5].