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Suppression of Short Channel Hump of nMOSFET Using NF_3-Added ILD HDP Process

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Introduction

As application of battery-operated machines such as hand-held computer and PDAs, demands of low power DRAMs gradually show upward curve. To extend battery lifetime, subthreshold property of peripheral MOSFET is determinant factor to reduce stand-by power consumption. Although STI (Shallow Trench Isolation) process has been widely used in high density DRAM integration due to its superior isolation property, it has suffered from short channel hump of nMOSFET. Previous papers revealed that short channel hump of nMOSFET was mainly attributed to STI corner round. Also, recent literature reports that short channel hump of nMOSFET is closely related to ILD(Inter Layer Dielectric) layers. However, this is not enough to fully explain its phenomena. In this paper, its relationship of short channel hump with ILD HDP layer is insensibly investigated and NF_3–added ILD HDP process is proposed to maintain both hump-free nMOSFET and high transistor performance, for the first time.

Experimental

The device used in this evaluation was fabricated using nMOSFET for peripheral devices of 0.15um-ruled DRAM. The front-end included features such as STI, HDP gap fill, shallow source/drain extensions with tilted halo implant and thermally grown gate oxide(65Å). $TiSi_2$ is selectively formed on poly and S/D regions using sidewall spacer. The metal stack consists of Ti/TiN/W/Ti/TiN/Al. The inter-layer dielectric (ILD) is planarized by HDP. Planarization is done with chemical-mechanical polishing (CMP). Finally, SiN layer is completely capped. Experiment is intentionally categorized into four processes: (i) conventional structure with LP-TEOS/LP-SiN sidewall spacer and normal HDP process($1\%H_2$) (ii) HDP process($0.5\%H_2$) (iii) sidewall spacer composed of only LP-SiN, to completely block the migration path to channel edge region (iv) with LP-TEOS/LP-SiN sidewall spacer and NF_3-added HDP .

Results and Discussion

From the viewpoint of migration path, its relationship of short channel hump with ILD HDP layer is schematically shown in Fig.1 Conventional structure with LP-TEOS sidewall spacer is compared to Type II structure, composed of only sidewall spacer SiN, in order to intentionally block the migration path to channel edge region as shown in Fig.2(b). I-V curve of split groups reveals that hump effect of Type III is considerably improved while a large magnitude of hump is observed in Type I. Also, short channel hump of nMOSFET is strongly dependent of hydrogen concentration in HDP layer. High temp annealing (500~800℃) with hydrogen in Si/SiO_2 interface could introduce a considerable fixed positive charge density in gate oxide [4]. HDP Process with low H_2 improves partially hump effects. Fig.5 presents subthreshold slope for nMOSFET having hump effect is degraded. Subthreshold variation is characterized through its relationship of S-factor with hump effect. Fig.6 shows junction reverse current in the gated diode structure as a function of Vgs. Surface generation current increased with increase of hump at Vds=0.3V, T=85℃. Surface generation current increased with the increase of hump magnitude. Judging from the aforementioned observations, HDP layer, containing a plenty of hydrogen, generates positive charge in oxide and deteriorates transistor performance.[5]. This is regarded as a probable candidate for an origin of hump happening. In order to reduce HDP-related hump effect, NF_3-added HDP process, incorporating appropriate amount of F, was suggested. In Fig.7, NF_3-added process surpasses Type III process, in regard to hump characteristics. It has been reported that fluorine interacts strongly with hydrogen in the film and catalytically removes the hydrogen from the system or deactivates the sites. In addition, the fluorinated device reduces the density of oxide charges, which may be attributed to the formation of Si-F bonds. When compared to Type III, the improved dielectric charge-to-breakdown characteristics (TDDB) for fluorinated device are shown in Fig.8. Observations for FN tunneling current and short channel margin indicate that F-incorporation thickens gate oxide and results in additional Vt (threshold voltage) increase.(Fig.9,10,11). Short channel hump of nMOSFET can be significantly improved by incorporating appropriate quantities of fluorine during ILD-HDP process.

Conclusions

Hump phenomena in the subthreshold region of short channel nMOSFET was intensively investigated. Short channel hump of nMOSFET was closely associated with ILD HDP layer and significantly improved by incorporating appropriate quantities of fluorine during ILD HDP process. Thus, we proposed NF_3 added HDP process to maintain hump-free nMOSFET without the degradation of dielectric characteristics , for the first time.

References

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[3] S.K. Lai, *et al.*, J.Appl.Phys., Vol.54, No.5, p.2540, 1983
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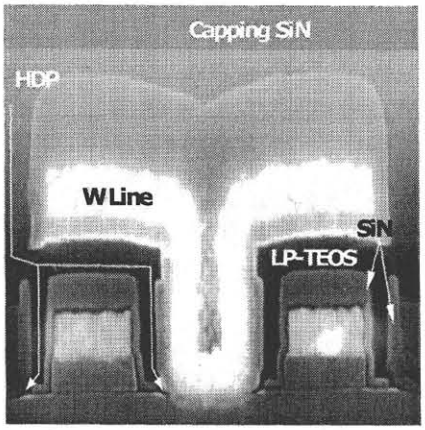
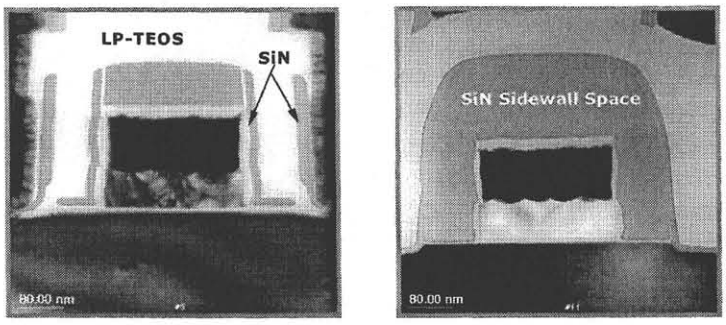


Fig. 1 SEM image of schematic cross sectional view. Si substrate is deliberately connected with ILD-HDP to characterize its relationship with hump.



(a) (b)

Split Condition	Gate Sidewall Spacer Layer	ILD-HDP
Type-I	LP-TEOS/LP-SiN	H_2-1%
Type-II	LP-TEOS/LP-SiN	H_2-0.5%
Type-III	LP-SiN	H_2-1%

Fig. 2. In order to verify ILD-HDP layer related hump, several experiments are intentionally considered. (a) conventional sidewall spacer structure (b) fully SiN-capped sidewall structure.

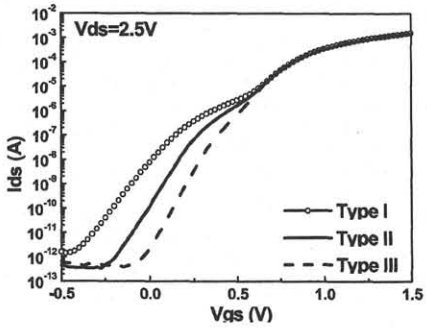


Fig. 3 Ids-Vgs curves of split groups show the hump phenomena depending on sidewall spacer type. A large hump effect at short channel MOSFET is observed in Type I structure.

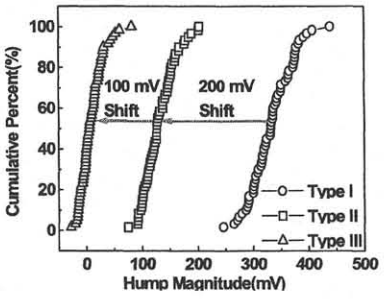


Fig. 4 Cumulative hump magnitude. Hump magnitude is defined as Vgs(@Ids=10nA) shift, in contrast to hump free I-V curve.

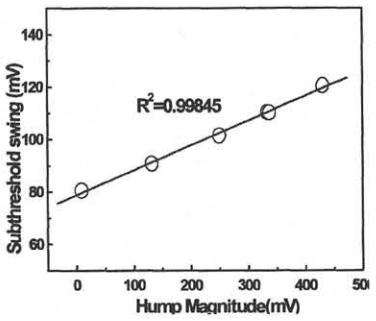


Fig. 5 Characterization of subthreshold swing as a function of hump magnitude.

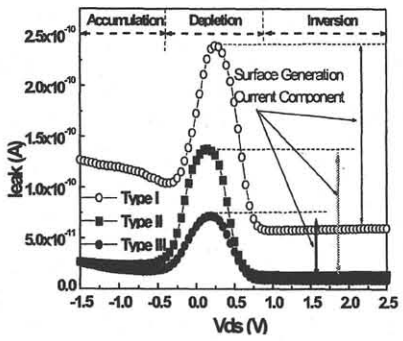


Fig. 6 Junction reverse current in the gated diode structure as a function of Vds. Surface generation current increases with increase of hump; Vds=0.3V, T=85℃.

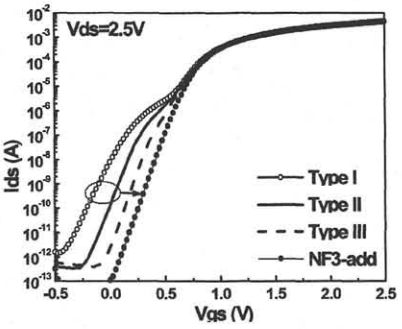


Fig. 7 nMOSFET with NF_3-added HDP film is superior hump effect to that of Type-III

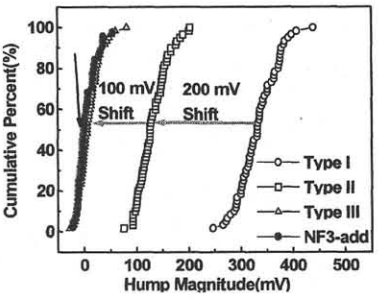


Fig. 8 NF3 added HDP process reduces hump magnitude, significantly.

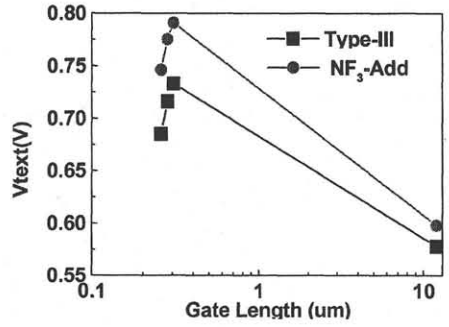


Fig. 9 Short channel margin for nMOSFET employing NF_3 added HDP process is comparable to Type-III.

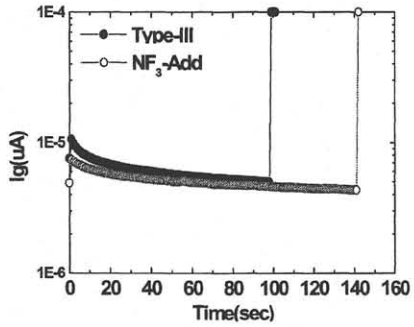


Fig.10 Comparison of TDDB (time dependant dielectric breakdown). NF_3 added HDP process is superior to Type-III.

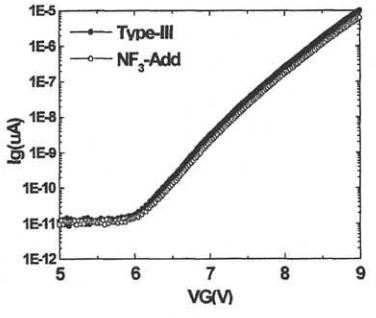


Fig. 11 Difference of FN tunneling current between NF3-added process and Type-III is not remarkable.