Impact of Thermal Budget Reduction on MOSFET Performance to Achieve High-speed and High-density DRAM-based System LSI

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1. Introduction

Demand for system LSI has increased recently for use in lots of different products, such as digital AV equipment and mobile phones. System LSI requires both high-performance logic and high-density embedded memory, as illustrated in Fig. 1. However, it is very difficult to fabricate a single chip that has both high-performance logic and high-density memory. This is because a conventional memory fabrication processes, especially capacitor proc-esses, require use of high temperatures after MOSFET fabrication, and such high temperatures lead to MOSFET degradation due to impurity deactivation. This can be avoided by fabricating embedded memory in a low-temperature process. In this paper, we describe an approach that allows fabrication of embedded memory at low temperature, using both a MIM (Ru/Ta₂O₅/Ru) capacitor [1] and low thermal budget SiN CVD. We demonstrated the impact of this low thermal budget process on MOSFET performance in an experiment.

2. DRAM Process Integration

Figure 2 shows a schematic drawing of a DRAM component after BL formation. A tungsten poly-metal gate [2] and tri-layer barrier metal technology for a tungsten contact [3] were employed. In order to create a self-aligned storage node contact, $LPCVD-Si_3N_4$ films with good step-coverage were used as an etching stopper for bit-line cap and sidewalls. Although use of LPCVD-Si_3N_4 is attractive because of its high step-coverage, its high-temperature and long-lasting thermal sequence increases the thermal budget drastically after final activation and degrades device performance. We overcame this problem by applying . low-temperature LPCVD-Si₃N₄ technology together with a hexachlorodisilane (HCD) gas source [4] instead of dichlorosilane (DCS), the conventional source, thereby successfully lowering the process temperature from more than 700°C to less than 650°C. Figure 3 shows the leakage current distribution between the BL and SN, measured using a 4M-bit test vehicle over the entire wafer to which the low-temperature HCD-Si₃N₄ was applied as an SAC etching stopper. No SN-BL short caused by the SAC process was observed, indicating the adequate selectivity of the HCD-Si₃N₄ film during SAC etching. Furthermore, the process temperature of capacitor formation was successfully lowered with Ru/Ta2O5/Ru MIM capacitor technology [1] keeping an adequate storage capacitance of more than 25fF/cell. A DRAM cell array containing the MIM capacitor is shown in Fig.4.

3. Thermal Budget Impact on Transistor Performance

The impact of lowering the process temperature was clarified by measuring peripheral devices with a 5.2-nm gate dielectric. Figure 5 shows the Ion vs. Ioff characteristics for both NMOS and PMOS at Vds=2.0 V under different thermal process temperatures. In this figure, less than 600°C means the maximum process temperature is limited because of the MIM Ta₂O₅ capacitor fabrication process, and more than 600°C indicates that the LPCVD-Si $_3N_4$ deposition process gives the highest temperature. Lowering

the process temperature was observed as having a strong impact on performance. By using 600°C as the process temperature, drive currents for both NMOS and PMOS at Ioff=10 pA/um improved by about 10% and 13%, respectively, compared to those for the conventional nitride process at 700°C. This seems to be mostly caused by improvement of dopant deactivation.

Figure 6 shows active contact resistance as a function of applied voltage. In the 700°C process, contact resistances to both N⁺ and P⁺ diffusions increased drastically as applied voltage decreased, that is, these contacts show strong non-linear characteristics even though a thermally stable metal contact process was implemented [4]. This non-linearity sometimes became a serious problem in circuit design. Since no $TiSi_x$ agglomeration or TiN barrier property problem was observed by TEM on the contact bottom, the non-linear characteristics originate from low active dopant concentration at the interface between the substrate and TiSix layer as a result of dopant deactivation or its absorption into TiSix. With the decrease of the process temperature from 700°C to less than 600°C, not only contact resistance but also its ohmic characteristics were improved significantly, resulting in less deterioration of transistor performance. Sheet resistances of N^+ and P^+ diffusions also indicate less dopant deactivation when a low-temperature process was used, as shown in Fig. 7.

 P^+ -poly gate depletion is another serious problem in dual work-function devices. Figure 8 shows C-V curves of PMOSFETs with L/W=100/100 um at different process temperatures. The 700°C process clearly indicates a higher poly depletion rate, and by lowering the temperature to below 650°C, effective oxide thickness was improved by about 0.4 nm.

Finally, in order to evaluate circuit performance for a low-temperature nitride process, the propagation delay time (T_{pd}) of an inverter ring oscillator was measured. Figure 9 shows T_{pd} as a function of F/O at Vcc=2.0 V. The gate length of MOSFETs in the inverter circuit was 0.16 um, and the maximum process temperature after final activation was 650°C. A time of 125 ps was obtained for T_{pd} of F/O=3 and this is fast enough for high-density DRAM-based system LSI.

4. Conclusion

We have clarified the impact of lower process temperatures on device performance. By applying low-temperature nitride deposition process and MIM capacitor formation process, deterioration of peripheral device performance was effectively suppressed; as a result, a time of 125 ps was obtained for T_{pd} of F/O=3. This technology is a promising candidate for application in fabricating future system LSI chips.

References

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Fig. 3 Distribution of leakage current between bit-line and storage node.

Fig. 4 TEM cross-sectional view of DRAM cell array.



Fig. 6 Contact resistance of (a) BL-N⁺ and (b) BL-P⁺ as a function of applied voltage under different SiN-CVD conditions. The contact size is 0.2 um^2 .



Fig. 8 C-V curves of boron-doped P⁺ polysilicon gate at different SiN-CVD conditions.

Fig. 5 Relationship between Ion and Ioff of (a) NMOSFET and (b) PMOSFET under different SiN-CVD conditions.



Fig. 7 Distribution of sheet resistance at (a) N^+ diff. and (b) P^+ diff. under different SiN-CVD conditions.



Fig. 9 Ring oscillator measurements. A 0.16-um MOSFET was used.