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Performance of DRAM Cell Transistor with TDSE (Thermal Desorption Silicon Etching) and Selective Si Channel Epi techniques

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1. Abstract

TDSE (Thermal Desorption Silicon Etching) process is introduced before Si channel-epi growth using UHV-SEG (Selective Epitaxial Growth) technique to improve transistor performance in DRAM device. Compared with the conventional channel-epi which shows the degradation of transistor characteristics due to the raised active profile, TDSE structure with channel-epi presents superior transistor performance in terms of transistor hump characteristics and inverse narrow width effect (INWE).

2. Introduction

Silicon SEG (Selective Epitaxial Growth) has been widely investigated in terms of device integrations and transistor performance [1-5]. Channel-epi engineering using SEG is one of the key technologies for improving the mobility and short channel effect of MOSFETs [6]. DRAM cell transistor with channel-epi, however, has not been studied in details. Raised active profile from channel-epi growth at small bar-type cell shows transistor hump at the edge of cell, which decreases threshold voltage (V_{th}) of cell transistor and eventually results in degradation of dynamic refresh characteristics in DRAM. To improve DRAM cell transistor, TDSE (Thermal Desorption Silicon Etching) technique has been developed and integrated with channel-epi for the first time. In this paper, the improved transistor characteristics with TDSE and channel-epi processes are described.

3. Experimental

DRAM FEOL (Front End Of Line) process flow is illustrated in Table 1. An STI process was performed for isolation. After wet cleaning, TDSE process was carried out using Cl_2 gas at 700 ℃ in UHV chamber. The process pressure was 10^{-6} torr. Following the TDSE process, *In-situ* Si channel-epi is grown at the same chamber. The selectively grown Si channel was doped by ion implantation through a sacrificial oxide layer. After the removal of sacrificial oxide layer, 5.5 nm of nitrided oxide was grown as a gate dieletric. For the formation of gate electrode, phosphorus doped polysilicon and WSi_x are sequentially grown on gate oxide. The lightly doped drain (LDD) and deep source/drain were formed by phosphorus and arsenic ion implantations, respectively.

4. Results and Discussion

Figure 1 shows the cross sectional SEM images of DRAM cell with conventional channel-epi and TDSE/ channel-epi. As shown in Figure 1, TDSE/ channel-epi technique can align Si epi surface with STI top surface, while conventional channel-epi results in raised active profile with strong Si (111) facet. Figure 2 is the distribution of V_{th} for three different cell transistors. TDSE/channel-epi transistor exhibits higher V_{th} of cell transistor compared to conventional channel-epi and reference (no channel-epi) cell transistors. The higher V_{th} for TDSE/channel-epi transistor may be attributed to active corner rounding formed by TDSE and SEG processes [7]. Shown in Figure 3 are the I_d-V_g characteristics for different back biases. Using TDSE/ channel-epi technique, the I_d-V_g characteristics for different back biases are significantly improved while conventional channel-epi transistor shows severe hump characteristics as back bias increases. Figure 4 is the V_{th} of core nMOSFETs for different gate lengths and active widths. As shown in Figure 4, less inverse narrow width effect (INWE) is identified for TDSE/ channel-epi transistor than for reference transistor (no channel epi). It can be also suggested that the improved INWE is ascribed to active corner rounding for core nMOSFETs. The N-/P-well junction leakage and Q_{bd} characteristics are depicted in Figure 5 and Figure 6, respectively. From the Figure 5 and 6, it is identified that both junction leakage and Q_{bd} characteristics are degraded by TDSE/channel-epi process. TEM image in Figure 7 suggests that the degradations of junction leakage and Q_{bd} characteristics may be related to the defects at channel epi/Si-substrate interface, which is originated from rough Si surface after TDSE process. Therefore, it is expected that the degradations of junction leakage and Q_{bd} characteristics can be improved by minimizing initial Si roughness before channel epi growth via H_2 added TDSE or H_2 annealing after TDSE process (Figure 8).

5. Conclusion

TDSE (Thermal Desorption Silicon Etching) process is introduced before Si channel-epi growth using UHV-SEG (Selective Epitaxial Growth) technique to improve transistor performance in DRAM device. Compared with the conventional channel-epi which shows the degradation of transistor characteristics due to the raised active profile, TDSE structure with channel-epi presents superior transistor performance in terms of transistor hump characteristics and inverse narrow width effect (INWE). In addition, it is suggested that the degradations of junction leakage and Q_{bd} characteristics can be improved by minimizing initial Si roughness before channel-epi growth via H_2 added TDSE or H_2 annealing after TDSE process.

References

[1] H. Koga et al., IEDM Tech. Dig., p.25, 1997.
[2] Satoshi Yamakawa et al., IEEE Electron Device Letters, 20(7), p.366, 1999.
[3] Emmanuel Augendre et al., IEEE Tran. Electron Devices, 47(7), p.1484, 2000.
[4] A. Hokazono et al., IEDM Tech. Dig., p.243, 2000.
[5] Yoshiki Kamata et al., Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, 2001, p.150, 2001.
[6] Kenji Noda et al., IEEE Tran. Electron Devices, 45(4), p.809, 1998.
[7] H. S. Uh et al., Symp on VLSI Tech., p.27, 2001.

- ○ Shallow trench isolation (STI)
- ○ ***Si 40nm etching by TDSE***
- ○ ***Si channel epi 40nm***
- ○ Channel ion implantation
- ○ Removing surface oxide
- ○ Gate oxidation (5.5 nm)
- ○ Gate Electrode formation
- ○ LDD formation
- ○ SiN spacer formation
- ○ Deep source/drain formation
- ○ Activation annealing
- ○ Metallization

Table 1. Process flow for DRAM fabrication.

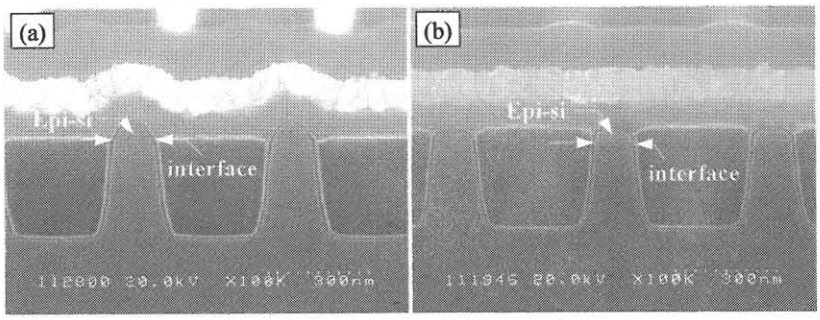

Fig. 1 SEM images of (a) conventional channel-epi, and (b) TDSE/channel -epi transistors.

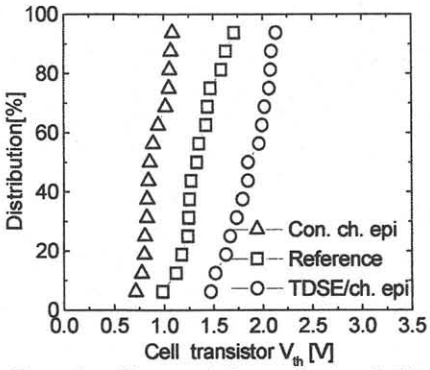

Fig. 2 Characteristics of threshold voltage of cell transistor. Reference indicates no channel-epi transistor.

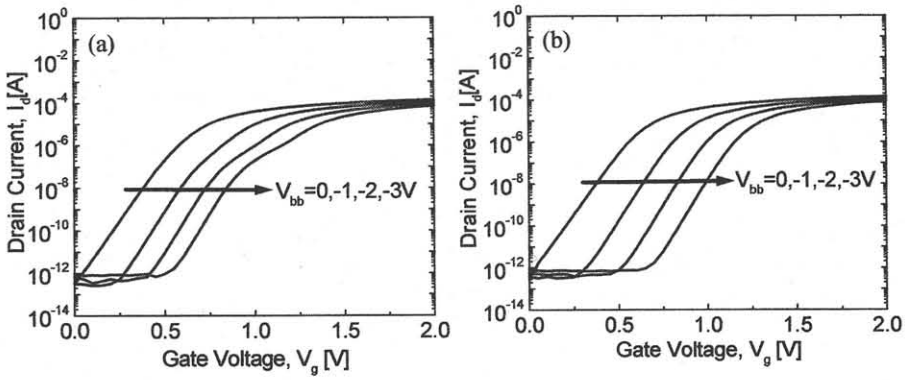

Fig. 3 I_d-V_g characteristics of (a) conventional channel-epi, and (b) TDSE/channel-epi transistors.

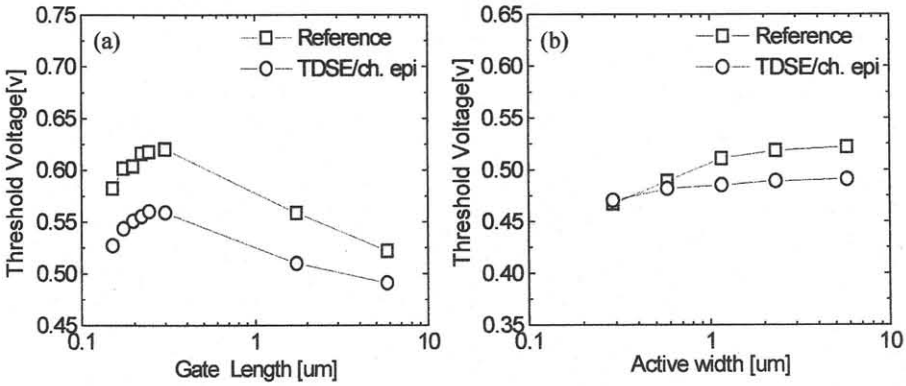

Fig. 4 V_{th} of core nMOSFETs for different (a) gate lengths, and (b) active widths.

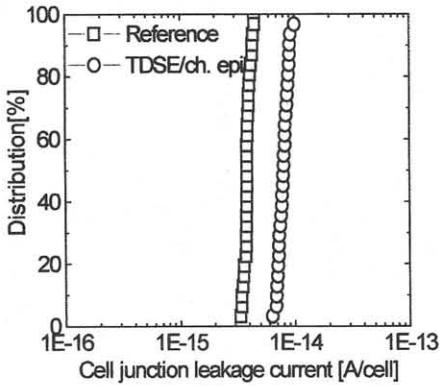

Fig. 5 N-/P-well junction leakage current.

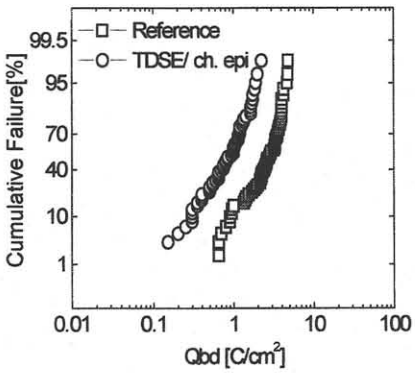

Fig. 6 Q_{bd} characteristics of nitrided gate oxide 5.5nm.

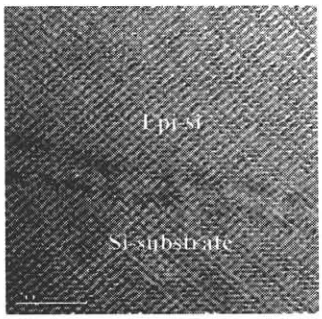

Fig. 7 TEM image of TDSE/channel-epi layer. The image shows defects at Si-substrate and epi-Si interface.

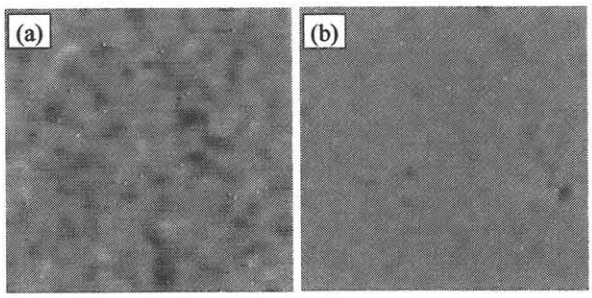

Fig. 8 Atomic force microscopic (AFM) view of Si surface (a) after TDSE (Cl_2)/channel-epi growth (RMS= 0.460nm), and (b) after TDSE (Cl_2+H_2)/channel-epi growth (RMS =0.356nm).