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Investigation of the Contact Resistance between Ru and Ti/TiN in M1/Plate Contacts of RIS (Ruthenium Insulator Silicon) Capacitor

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1. Introduction

The implementation of the noble metals for the electrodes in MIS (Metal Insulator Silicon) and MIM (Metal Insulator Metal) capacitor is becoming more necessary in order to increase the capacitance of DRAM below 0.1㎛ technology. One of the most promising candidates for the noble metal electrode is ruthenium (Ru) due to the availability of CVD process, relatively easy dry etching characteristics and excellent capacitor electrical properties [1].

However, there are many issues to be solved for the complete integration of Ru electrode in capacitor. One of the problems is the poor adhesion between Ru top electrode and ILD. In order to alleviate the adhesion issue, a capping layer such as Ta_2O_5 is needed on Ru. Although the implementation of Ta_2O_5 capping layer can solve the adhesion issue, it gives a rise to an additional issue of metal to plate contacts (M1/Plate). The contact resistance characteristics of Ru and titanium (Ti) is yet to be understood. In this study, we investigated the contact resistance of Ru and Ti/TiN in M1/Plate contacts in full integrated DRAM with a RIS (Ruthenium Insulator Silicon) capacitor.

2. Experimental

Ta_2O_5 insulator and Ru top electrode were deposited by MOCVD process[1]. On the Ru top electrode, Ta_2O_5 was deposited with O_2 reactant as a capping layer for the purpose of an adhesion layer. After patterning the metal contacts (A/R : metal-1/bit-line $\geq$ 10, metal-1/Ru $\geq$ 7), Ti/TiN barrier metals were deposited with PVD and CVD processes. CVD-Ti/TiN fillms were deposited by $TiCl_4$-based PECVD-Ti in H_2 plasma environment. PVD-Ti/TiN films were deposited with i-PVD process in order to enhance the step coverage. The plug fill for the metal contact was carried out by PMD-Al process which has been developed for complete filling of deep and small contacts by CVD-Al process[2,3]. For the measurement of contact resistance, 1000 contact string patterns were used. The effects of PVD and CVD-Ti/TiN barriers were compared by electrical measurements of the string contacts in M1/Plate contacts on Ru and M1/BL (Bit Line) contacts on W bit-line. The interface qualities between Ti and Ru were evaluated by TEM, and the chemical composition was analyzed by AES and XPS. Fig. 1 is the schematic diagram of the tested structure with RIS capacitor and Ru to Ti/TiN contacts in M1/Plate.

3. Results and Discussions

Fig. 2 shows the contact resistances for the M1/Plate contacts on Ru and the M1/BL contacts on W bit-line with different ohmic and barrier metals. With PVD-Ti/TiN barrier, extremely high values of contact resistance were measured at Metal-1/Ru contact. The contact resistance with PVD-Ti/TiN ranged from 5,000 to 10,000 Ω/CNT. On the other hand, with CVD-Ti/TiN bilayer, a low resistance of 15Ω/CNT was measured. The possible cause of the high contact resistance on M1/Ru contact with PVD-Ti/TiN barrier can be explained by as follows. One is the formation of void at M1/Ru contact with PVD-Ti/TiN and PMD-Al process. Another possibility is a formation of a highly resistive compound at the contact.

The TEM in Fig. 3 shows complete fill of a 0.2㎛ M1/Ru contact with aspect ratio of 7 using the PVD barriers. Therefore, it is assumed that void is not the root cause of the high contact resistance on M1/Ru contact. Besides, in the case of the resistance of M1/BL contact with higher A/R, there was no difference between two types of barrier layers (Fig.2(b)).

The TEM images of the interface between Ru and Ti/TiN with PVD and CVD barriers are shown in Fig. 4. With CVD-Ti/TiN barrier, a clean interface was observed without the formation of any interfacial layer. However, with PVD-Ti/TiN barrier, 45Å-thick layer at the interface was observed. The chemical composition of the interfacial layer in Fig. 4(b) was analyzed by XPS. Fig. 5 shows the O_{1s} spectra of the interfacial layer consists of a peak at 531eV which is attributed to TiO_x[4]. Therefore the high contact resistance of M1/Plate contacts with PVD-Ti/TiN barrier is due to the formation of titanium oxide at the interface.

The result of XPS is reconfirmed by comparing the AES depth profiles of the Ru and Ti interface. Two kinds of Ti/TiN stacks (PVD-Ti/TiN, CVD-Ti/TiN) were deposited on Ru, which contained the residual oxygen. In Fig. 6, the AES depth profile showed a high oxygen content between Ru and TiN in case of the PVD-Ti/TiN barrier. Since the Ti profile overlaps with the oxygen profile, the existence of TiOx layer is reconfirmed. On the contrary, oxygen was not detected in the case of CVD-Ti/TiN process. It is believed that the residual oxygen content in Ru was decreased with PECVD-Ti process. Since PECVD-Ti process is carried out in reducing H_2 plasma environment, the oxygen content of the underlayer can be reduced. To investigate the effect of H_2 plasma for decreasing the oxygen content in Ru, PVD-Ti/TiN was deposited onto oxidized Ru after H_2 plasma treatment. AES depth profile (Fig. 6 (c)) shows that oxygen content was dramatically reduced with H_2 plasma treatment, presumably due to the reducing ability of H_2 plasma. Besides the existence of oxygen rich layer can be prevented by the in-situ post nitridation The noticeable difference between PVD and CVD-Ti/TiN was that there was no metallic Ti layer in the case of CVD-Ti/TiN process. The lack of Ti layer with PECVD-Ti can be explained by the in-situ post nitridation step of the PECVD-Ti process which is carried out after the deposition of Ti. it is believed that PECVD-Ti films are completely changed to TiN after the post nitridation. Because TiN is much more resistant to oxidation in comparison to the metallic Ti, the formation of highly resistive TiOx layer can be prevented when PECVD-Ti barrier is used.

Therefore, in order to prevent the oxidation of Ti layer on Ru plate, the implementation of CVD-Ti/TiN process is necessary. With CVD-Ti/TiN, a successful integration of

metal-1 and Ru top electrode was achieved with low contact resistance.

4. Conclusions

A successful integration of metal contact and Ru top electrode is achieved by using CVD-Ti/TiN barrier in M1/plate contacts. PVD-Ti/TiN process resulted in a high contact resistance because of the oxidation of Ti due to the residual oxygen content in Ru top electrode. The formation of titanium oxide interfacial layer was completely prevented with CVD-Ti/TiN due to oxygen-reducing H_2 plasma environment and the nitridation effect of the in-situ post nitridation.

References

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[3] J. M. Lee, et al., The International Interconnect Technology Conference, 2001, p. 72

[4] K. Tanaka, et al., Applied Surface Science, 171, 2001, p. 71

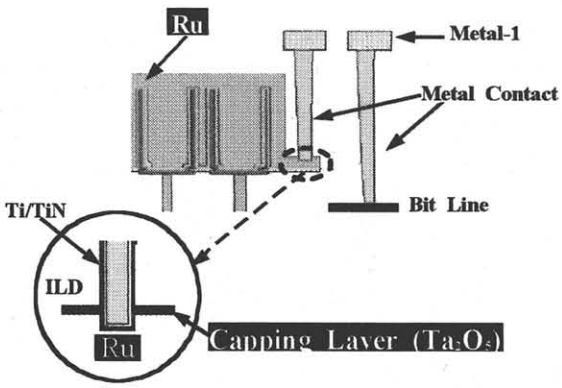

Fig. 1. Schematic cross section of the tested structure with RIS (Ruthenium Insulator Silicon) capacitor with Ta_2O_5 capacitor and capping layer

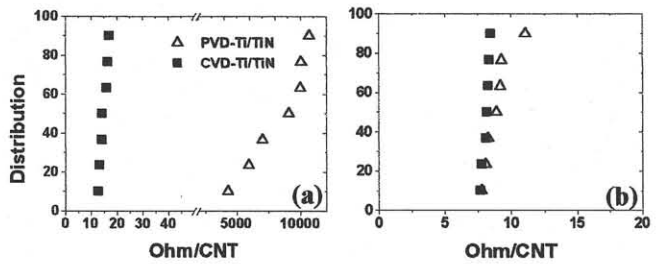

Fig. 2. Metal contact resistance (@ 0.2㎛) (a) Metal-1/Ru, (b) Metal-1/BL

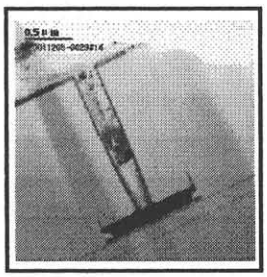

Fig. 3. TEM photographs of M-1/Ru contact cross-sections showing void free fill with PVD-Ti/TiN.

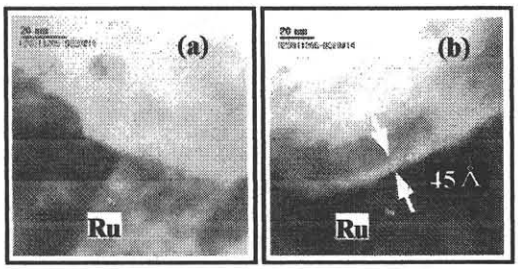

Fig. 4. TEM photographs of the interface of Ti and Ru (a) CVD Ti/TiN, (b) PVD Ti/TiN

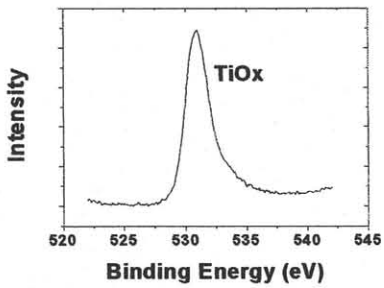

Fig. 5. O_{1S} XPS spectrum of Ti layer in Ru/Oxidation/ PVD Ti/TiN structure

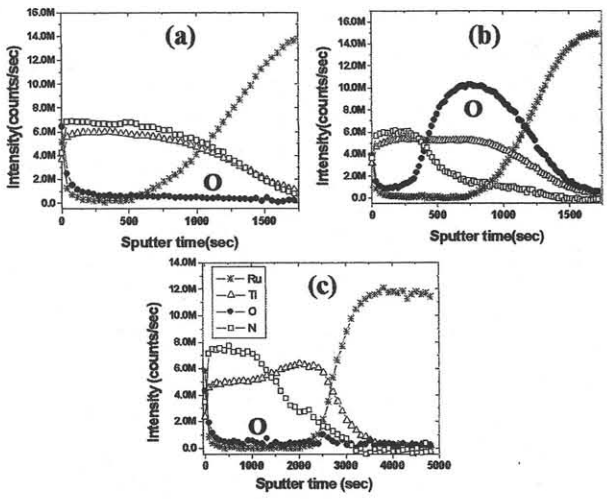

Fig. 6. AES depth profile of oxidized Ru/Ti/TiN stacks (a) CVD Ti/TiN, (b) PVD Ti/TiN, (c) PVD Ti/TiN (H_2 plasma treatment)