Lattice Strain in Scaled Devices Revealed by Using Convergent-Beam Electron Diffraction

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1. Introduction Lattice strain in a semiconductor device has been suggested as a cause of degradation of device performance [1,2]. We have reported that shallow trench isolation (STI) can cause serious local lattice strain and can produce crystal defects in a substrate [3]. However, in scaled devices, the other device components, such as the gate-stack structure, can also be sources of lattice strain, which in turn affects the device performance. The experimental examination of the strain due to those components in scaled devices has not yet been reported.

Accordingly, we used convergent-beam electron diffraction (CBED) to experimentally examine the lattice strain caused by those components. CBED is the only method that can experimentally measure the local lattice in a scaled device (0.13- μ m rule): it provides 10-nm spatial resolution and detects strain of 2×10⁻⁴. Our examination shows that lattice strain in the channel regions is largely affected by the components above the channel as well as the STI. This indicates that the strain must be controlled to improve transconductance in MOS devices.

2. Local lattice strain measurements by CBED Figure 1 shows the principle of CBED. The incident electron is focused on a spot on the specimen. CBED has much higher spatial resolution than the conventional lattice strain measurement methods, such as micro-Raman spectroscopy and x-ray diffraction. In this study, the electron probe diameter was about 20 nm. The standard deviation of the measured strain was 2.0×10^{-4} .

Corresponding to the diffracted electron, the deficient lines, so called Higher-order Laue zone (HOLZ) lines are generated in the transmitted disk. The lattice strain in the illuminated region is extracted from the variation of the positions of HOLZ lines. An example of transmitted disk is shown in Fig. 1. The details of the lattice strain measurement method were reported in Ref. [4].

3. Local lattice strain in scaled devices We classified the strain sources in scaled devices into the following four groups: 1. isolations, 2. components making contact with device region, 3. thin films having no contact with the device region, and 4. thermal annealing.

Figure 2(b) shows the strain distribution in a scaled device such as that depicted in Fig. 2(a). The measuring positions (horizontal axis) correspond to the numbers indicated in Fig. 2(a). The strains in the horizontal direction

are shown. The strain at the positions 1-6 was caused by STI. The second kind of strain source gives the strain locally near the contact point, such as the interface between the plug and the substrate surface. In Fig. 2(b), large strains and their variations are observed near position 11, where the plug and substrate surface make contact. The third strain source exerts a uniform strain contrary to the second kind of strain source. Figure 3(b) shows the strain distributions in the case of W/WN/poly-Si gate stack (filled circle) and WSi/poly-Si gate stack (open circle), respectively. It was found that the sign of the strain beneath the gate stack changed due to the difference of the gate-stack materials. Thermal annealing also affects the strain. Figure 3(c) shows the strain distributions of the specimen (same structure as that shown in Fig. 3(a)) without anneal (filled circle) and annealed after gate-stack fabrication.

Figure 4 shows a comparison between the STI strain and the strain variation induced by the above strain sources. Each source can change the strain in the same order as STI strain. Thus, it is possible to affect the performance of the device. For example, the 1×10^{-3} strain in the direction perpendicular to the channel leads to about a 3% transconductance deviation in a pMOS [5]. Therefore, to realize excellent device performances, it is indispensable to control the strain induced by not only STI but also by the other strain sources.

4. Conclusions Strain distributions in scaled devices were revealed in nanometer scale by CBED. The contact plug, the kinds of gate-stack materials, the annealing process as well as STI can cause the strain variation enough to change the transconductance. Nanometer-scale strain measurements by CBED and strain control are indispensable for the improvement of scaled device fabrication processes.

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6. References

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of HOLZ pattern (right).





Fig. 2 (a) Schematic of the comparison between the dimensions of the scaled ULSI devices and the probe diameter of CBED.(b) The strain distribution in a scaled device such as (a). The positions (horizontal axis) correspond to those in (a).



Fig. 3 (a) Schematic of the specimen in which CBED was conducted. (b) The strain distribution in the case of W/WN/poly-Si gate stack (filled circle) and WSi/poly-Si gate stack (open circle). (c) The strain distribution of the specimen without annealing (filled circle) and with gate annealing (open circle).

Fig. 4 Comparison between STI strain and the strain variations induced by contact plug, the kinds of gate-stack materials, and annealing process. Each process caused the strain variation in the same order as STI strain. Right axis shows the corresponding transconductance deviation in pMOS for the strain perpendicular to the channel direction (corresponding to Fig. 3)[5].