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High-Resolution Compositional Profiling of High-κ Gate Stack Structures.

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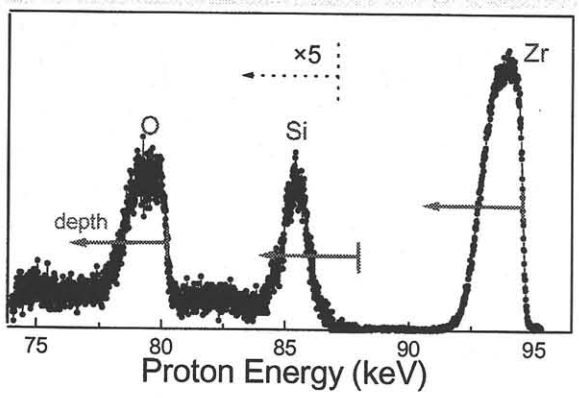
As the art of ultrathin (0-10nm) film design and fabrication is converted into a science, the necessity of accurate compositional depth profiling has grown more important. Technical need is quite diverse and includes applications in tribology, corrosion, catalysis, lubrication, photonics, and perhaps most important, microelectronics. A variety of experimental tools are now available to offer information about composition, as well as structural, vibrational and electronic properties of ultrathin films. Methods to deduce elemental composition include variants of ion scattering, electron spectroscopy, electron microscopy and optical spectroscopy. In practice, a full characterization usually requires that one go beyond a simple compositional analysis to fully understand and predict film behavior.

In microelectronics, substantial technical barriers have arisen in the continuous decrease in device size (scaling). Arguably the most critical problem concerns the gate dielectric, in which current leakage via tunneling through SiO_2-based films with thickness of less than 1.5nm is rapidly becoming too high to yield a practical device. One solution to this problem involves the replacement of SiO_2 with a higher permittivity metal oxide dielectric. In this presentation, we review the methods that are used to yield information about gate stack structures, concentrating on medium energy ion scattering (MEIS) studies of high-κ metal oxide dielectrics. The issues addressed go well beyond compositional profiling and include the materials chemistry of growth and layering methods, high temperature film breakdown, and more generally, the thermodynamics and kinetics of ultrathin high-κ gate stack structures. We also discuss the correlation between atomic scale physical properties and device electrical behavior.

Careful MEIS analysis (using H nuclei of energy ~100keV) permits an absolute quantification of elements contained in thin films (due to the Rutherford-dependence of the scattering cross section). The use of stopping power and straggling data, which are well established in this energy range, furthermore allows one to extract elemental depth profiles from the energy spectra of most elements contained in thin high-κ films. To convert the areal density profiles (in units of atoms/cm^2) into nm-scale depth profiles, knowledge of the density of the layer is needed. In optimal cases a depth resolution of 0.4nm for near-surface layers can be obtained that deteriorates to 1nm for layers buried at a depth of 5nm. In Fig. 1 we present typical ion scattering data for an ultrathin film of $ZrO_2/SiO_2/Si$ with a ZrO_2 film thickness of ~3.5nm and an SiO_2 interface thickness of ~0.8nm.

Fig. 1 MEIS ion scattering yield for a ZrO_2(3.5nm)/SiO_2(0.8nm)/Si.stack



Many potential high-κ gate dielectric materials react with elemental silicon in the gate electrode or the channel under realistic processing conditions. Such materials may require an interfacial layer to improve interface electrical properties or to act as a thermal diffusion barrier. Although SiO_2 or SiO_xN_y may seem logical choices, if the interfacial barrier layer is either of these (or another low permittivity material) it will significantly limit the maximum achievable capacitance. It is thus important to have a detailed understanding of the thermal stability of high permittivity materials on silicon, both with and without interfacial layers. In standard MOSFET processing, the gate stack must withstand temperatures >1000°C.

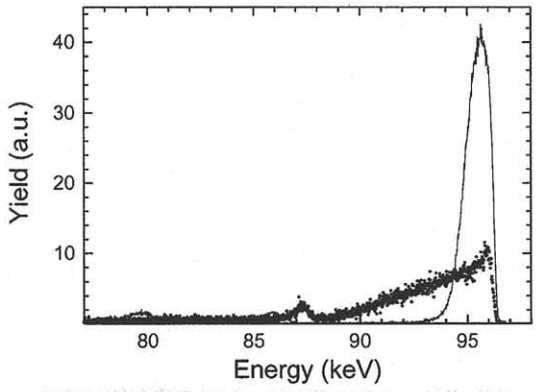


Fig. 2 MEIS ion scattering yield from HfO2 film before and after thermal decomposition in vacuum

Using high-κ films produced by CVD, ALD and PVD methods, we have used medium energy ion scattering (MEIS) to study the thermal integrity of single and multilayer stacks at temperatures up to 1000°C. In Fig. 2 is presented MEIS data for an $HfO_2/SiO_2/Si$ stack that has been annealed to 1050°C in UHV for one minute. MEIS analysis of the films show Hf silicide formation is observed above 1000°C as the HfO_2 decomposes. In this study the thicknesses of both SiO_2 and HfO_2 layers were varied to develop a picture of film decomposition. Somewhat surprisingly, the dependence on SiO_2 layer thickness appears to be quite small, suggesting that the HfO_2 layer thickness is rate limiting in this thickness regime.

For a number of different systems (M = Zr, Hf, Y, La, Gd...), our results support a picture in which high-κ gate stack decomposition occurs via SiO desorption and silicide island growth. The overall decomposition process can be written as:

$$MO_2 + SiO_2 + Si \rightarrow MSi_x + SiO\ (g)$$

Other interesting phenomena were observed and will be discussed in the presentation, including oxygen diffusion (examined by isotopic methods), oxide and silicide crystallization, and differences in the relative rates of SiO_2 and metal oxide reduction. This work was supported by the Semiconductor Research Corporation and the National Science Foundation (US).