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Performance and Time-dependent Degradation in a Single Grain-size Pentacene TFTs

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1. Introduction

Versatile advantages like low cost processing and mechanical flexibility make organic devices very attractive for enabling electron devices in the next generation[1,2]. Above all, pentacene ($C_{22}H_{14}$) is a promising material because it has been reported that its TFT has a relatively high mobility[1]. On the other hand, organic TFTs also need to be integrated for any practical application. However, a miniaturization capability of pentacene TFT has never been reported yet. This paper describes fabrication, performance and concerns about a single grain size pentacene TFT for the first time.

2. Device Fabrication

TFTs were fabricated on 33nm-thick SiO_2 thermally grown on heavily doped n^+ silicon wafer as shown in Fig.1. The heavily doped silicon substrate acts as the gate electrode. First, sub-μm spaced source/drain electrode patterns were defined by an electron beam lithography on the resist. Then Au was evaporated on it and lifted off for active area formation. Pentacene was grown by vacuum evaporation under base pressure of about 10^{-5} Pa, deposition rate of 0.05nm/s and substrate temperature of 25℃. The device reported in this paper has approximately 50nm-thick pentacene film, and 20-30nm-thick Au electrodes. Electrical characteristics were measured in an ambient atmosphere.
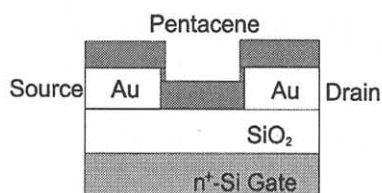

Fig.1. Schematic diagram of pentacene TFT device. The n^+ silicon was used for gate electrode, while the thermally grown SiO_2 was used for gate insulator. Pentacene was deposited on Au source/drain electrodes. The channel lengths are 0.2μm-10μm.

3. Results and Discussion
3.1. Short channel effect

Figure 2 shows an SEM image of channel region of L=0.2μm pentacene TFT in which the channel length is comparable to a single grain size. The normalized saturation current increases linearly with $1/L$ as shown in Fig.3. It indicates that the pentacene TFT can potentially be scaled to the grain size. On the other hand, a long channel device (L=10μm) shows an excellent on/off ratio of 10^6, however a short channel one (L=0.2μm) shows a poor on/off ratio of

$10^{1.5}$ as shown in Fig.4. It is so called the short channel effect (SCE) in the semiconductor device sense. Furthermore, it is noted that the short channel device shows a large hysteresis in the voltage sweeping. This hysteresis might be related to a time dependent degradation, which is next discussed in detail.
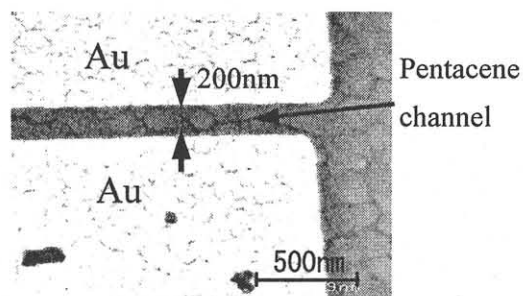

Fig.2. SEM image of L=0.2μm channel length pentacene TFT. The channel length is comparable to a single grain size.
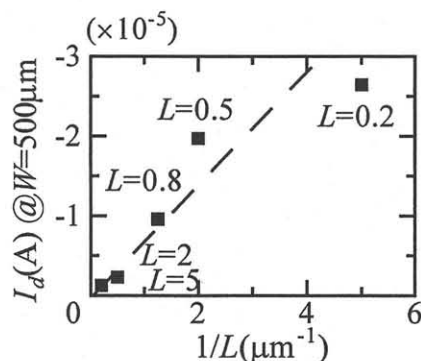

Fig.3. The channel length dependence of the saturation current, which are normalized at W=500μm. The saturation current increases linearly with $1/L$.
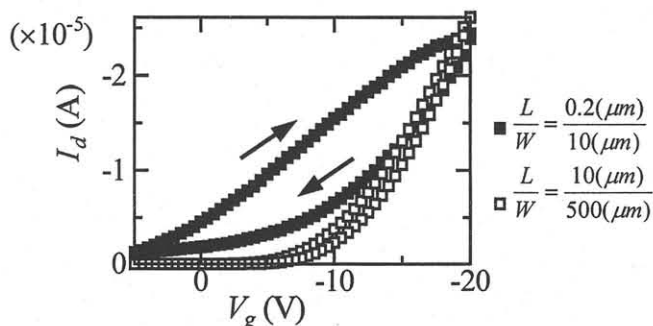

Fig.4. I_d-V_g characteristics of L=10, W=500μm (□) and L=0.2, W=10μm (■) pentacene TFTs. The voltage was swept from V_g =5V to –20V and from –20V to 5V. Large hysteresis is observed in L=0.2μm.

3.2. Hysteresis and time-dependent degradation

The hysteresis observed in I_d-V_g characteristic is enhanced with the channel length decrease. To analyze this, a channel length dependence of the hysteresis was investigated, as shown in Fig.5. Here, the hysteresis is defined as a half-width of full maximum in the drain current at V_d=V_g= -20. This fact suggests that large hystereses observed in sub-micron devices are due to the strong lateral electric field.

To determine what parameter is a dominant factor on the hysteresis, V_g and V_d dependent degradations were measured. Figures 6(a) and 6(b) show V_g and V_d dependent drain current degradations, respectively. The devices were left unbiased for 1.5 hours in the interval of each measurement, because the device performance almost returned to a stable state after an hour. In both cases, $I_d(t)$ can be described by the power of t as follows,

$$I_d(t) \cong A \cdot t^{\alpha}$$

,where $\alpha \cong -0.4$ in both cases. These results imply that an electrically stressed degradation mechanism is the same for changing V_d and V_g.

The recovery process is also important to clarify the degradation mechanism. Figure 7 shows the drain current degradations for several intervals. Namely, first, applying V_d=V_g= -10 for 1 minute, followed by zero-biased (□) or reversely biased (■) for 1 minute. This bias cycle was repeated five times. The results obviously indicate that this is not a permanent degradation but a recoverable one, and a better recovery is achieved in the reversely biased case.

Those degradations might be explained by following mechanisms: 1) the field induced ion drift in thin films[3], 2) trapping/detrapping of charges[4]. The ion drift in the film makes an internal opposite field against the external field, so the effective electric field can be reduced. On the other hand, when carriers are trapped in the defects, the local potential barrier in the channel may be created. Detrapping process works in the opposite way. Considering the ion drift might be a slow process, the fact that hysteresis appears within a short time (1-2 min.) suggest that the charge trapping/detrapping would be dominant in the drain current degradation. Although the reality of defects for trapping/detrapping is still unclear, it is mandatory to
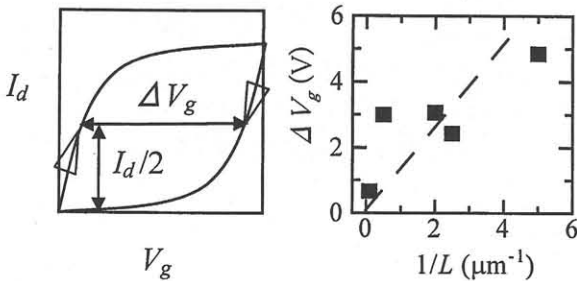

Fig.5. Channel length dependence of the hysteresis. Hysteresis was defined at half-width of maximum drain current (left diagram) biasing V_d=V_g= -20. As the channel length decreases, the hysteresis increases linearly.
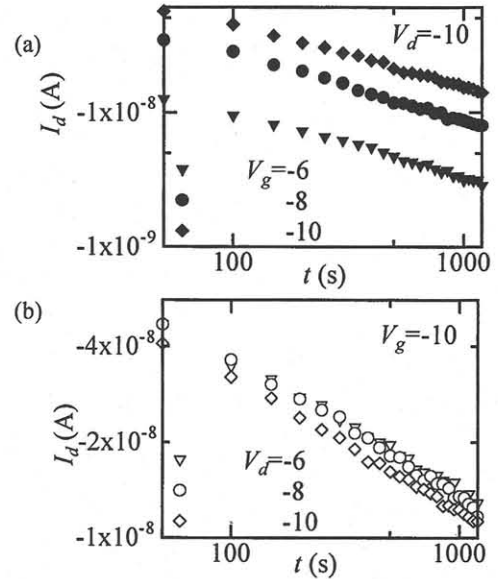

Fig.6. Log-log plots of (a) V_g and (b) V_d dependence of the drain current degradation of L=1, W=10µm pentacene TFT. From fitting to a power low curve, I_d=$A \cdot t^{\alpha}$ (α is about -0.4) is obtained.

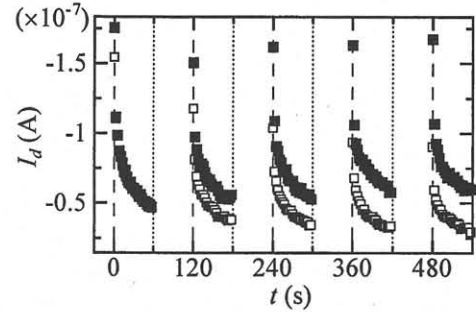**Fig.7.** Time dependent drain current degradation of the TFT left in zero-biased (□) and reversely-biased (■) states during each stressing experiment.

understand and overcome those challenges for achieving very short channel organic TFTs.

4. Summary

Electrical characteristics of a single grain size pentacene TFT were investigated. We have clarified that the pentacene TFT can be scaled to a sub-µm grain size. But the short channel effects must be suppressed for further miniaturization. Degradation and hysteresis are considered from the viewpoint of charging effect or ion drift, and it has been inferred that the charging effect might be dominant. Thus, it is concluded that overcoming those challenges are essential for further miniaturization of organic TFTs.

References
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