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Mechanism of Low-voltage operation in the Organic FET with the Top-and-Bottom Contact (TBC) Structure

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1. Introduction

In recent ten years, there have been remarkable developments in the organic electronics. Especially, organic field effect transistors (OFETs) have been intensively investigated in order to realize practical organic electronic devices [1], [2]. Employing organic materials allows us to fabricate low-cost, low-weight, printable, and flexible devices [3]. However, potential low mobility of organic semiconductor materials, comparing to that in inorganic semiconductor such as silicon, limits the range of practical use. To compensate the characteristic of organic semiconductor materials, structural factors in FET should be necessarily improved.

Recently, we have developed a new structured organic field effect transistor (FET), we called it Top-and-Bottom Contact (TBC) structure, which is prepared by a simple stacking process. The most remarkable advantage of employing the TBC structure is very short channel length by controlling the thickness of semiconductor layer. Even sub- μ m order of channel length can be easily prepared without any micromachining or related photolithography procedures.

In this study, we have prepared the TBC type organic FET (TBC-FET) with a very short channel length using pentacene and show the transistor properties peculiar to the TBC-FET. The mechanism of such a very low voltage operation in TBC-FET has been considered in relation to its unique structure.

2. Experimental

Fig.1 shows the cross-sectional illustration of our newly developed TBC-FET structure which was fabricated as following procedure. Heavily doped Si with thermally grown SiO₂ (300nm) was employed as a substrate and a gate electrode. Substrates were carefully UV-ozone cleaned before the fabrication of FET devices. Pentacene was train-sublimated 5 times for purification. An Au bottom electrode (250 nm) was deposited through the metal mask. On the bottom electrode a pentacene film (500 nm which is corresponding to the channel length) was deposited. After that, an Au top electrode (50 nm) was deposited onto the pentacene thin film surface. All thin film depositions are carried out by using thermal evaporation method at a pressure of ca. 10^{-6} Torr (deposition rate = $0.1 \sim 0.2$ nm/s). Electrical measurements were carried out by using a source meter (Keithley 2420) and a voltage source (Kepco ABC125-1DM).



Channel length≈Thickness of semiconductor layer

Fig.1 The cross-sectional illustration of TBC FET.



Fig.2 AFM image of pentacene film surface on the edge of bottom electrode.

3. Results and Discussions

Fig.2 shows AFM image of pentacene film surface on the bottom electrode. Since the evaporation source was located vertically below the substrate, it seems to be difficult to form the pentacene layer at the side of the electrode that has relatively sharp edge as shown in Fig.2. Then, in this study, relatively thick pentancene layer was deposited on the electrode in order to avoid short circuits in the device at electrical measurements. Although the thickness of pentacene layer is controllable for shortening the channel length, the optimum film thickness has to be arranged in this device.

 I_{DS} - V_{DS} properties of TBCFET are shown in Fig.3. I_{DS} is modulated by V_G . Besides the clear saturation behavior is observed in very low V_{DS} region from 0 to 5 V. However, I_{DS} begins to increase steeply at the high V_{DS} region, and then the operation tends to be unstable. This means that transistor properties can't be controllable at these high V_{DS} region for the TBC-FET.

From these results, the operation mechanism of TBCFET is suggested as shown in Fig.4 The low-voltage saturation indicates that the very short channel length is formed due to employ the TBC structure. According to the illustration in Fig.4, the line AC and BC represent the thickness of pentacene layer and the effective channel length, respectively. Thus, actually the channel length would be shorter than the thickness of pentacene layer (0.5µm). In low V_{DS} region, I_{channel} flows preferentially through the BC channel. Thus, with the increase of V_G a channel is generated on the BC line, and then I_{DS} is modulated. This behavior is substantially similar to that of the lateral-type FET. However, in the high VDS region, since the Ibulk steeply increased, the IDS is observed as the summation of Ichannel and Ibulk. In other words, the diode behavior begins to appear rather than the transistor behavior in the high V_{DS} region owing to such a vertical-type structure. This diode component will cause



Fig.3 Ins-Vns curves of amorphous pentacene TBCFET.

Low V_{DS} region



Middle and High V_{DS} region



Fig.4. The schematic illustration of the mechanism of transistor operation in TBCFET.

the decrease of Ion/off. In order to reduce the diode component, we have examined to form the Schottky junction with pentacene as the source electrode. Moreover, we have confirmed the high-performance operation in P3HT TBCFET. The detailed results for these devices will be shown on the presentation day.

4. Conclusions

We have succeeded in fabricating the high-performance TBCFET with a very short channel length (less than 0.5 μ m) by a simple stacking process, and demonstrated excellent performance at a low driving voltage. We also have clarified the mechanism of low-voltage operation in the TBCFET.

References

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