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Methodology for Accurate C-V Measurement of Gate Insulators below 1.5nm EOT

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Abstract
The gate capacitance (C) of MOSFET has been extracted from impedance measurement at a given frequency (ω: typically < 1MHz) based on an assumed equivalent circuit model (usually parallel model (PM): a capacitor (C) in parallel with a resistor (R)). However, recent aggressive scaling of gate insulator thickness causes the drastic decrease of impedance of the insulator and the shift of ωm to much higher ω, where ωm is the frequency giving the maximum amplitude of imaginary part of impedance (Im(Z)). Therefore, parasitic impedance elements cause serious errors especially below 1MHz. To reduce the effects of the parasitic impedance, C is calculated from Im(Z) at ωm which is searched by ω-sweep measurement [1] and PM have been extended into 3-element circuit model (3ECM) with well resistance in series (Rσ) [1-3]. Other models considering channel resistance [4-6] or built-in series inductance (L) [7] were also proposed. However, the measurement setups, which may cause the significant errors, were not considered properly in Ref.[1-7]. In this paper, we study the influence of the conventional configuration on C measurements and introduce another one which can extend the measurement frequency range (up to 100MHz) and reduce the parasitic impedance in the instruments.

1. Introduction
The gate capacitance (C) of MOSFET has been extracted from impedance measurement at a given frequency (ω: typically < 1MHz) based on an assumed equivalent circuit model (usually parallel model (PM): a capacitor (C) in parallel with a resistor (Rσ)). However, recent aggressive scaling of gate insulator thickness causes the drastic decrease of impedance of the insulator and the shift of ωm to much higher ω, where ωm is the frequency giving the maximum amplitude of imaginary part of impedance (Im(Z)). Therefore, parasitic impedance elements cause serious errors especially below 1MHz. To reduce the effects of the parasitic impedance, C is calculated from Im(Z) at ωm which is searched by ω-sweep measurement [1] and PM have been extended into 3-element circuit model (3ECM) with well resistance in series (Rσ) [1-3]. Other models considering channel resistance [4-6] or built-in series inductance (L) [7] were also proposed. However, the measurement setups, which may cause the significant errors, were not considered properly in Ref.[1-7]. In this paper, we study the influence of the conventional configuration on C measurements and introduce another one which can extend the measurement frequency range (up to 100MHz) and reduce the parasitic impedance in the instruments.

2. Experimental
n-MOSFET's with various gate sizes (typically 5-200um²) and with the gate insulators of Silicononxynitride thin films (< 2nm) were fabricated. Impedance measurements were made on a manual prober using Agilent 4294A impedance-meter in two methods. The first (usual) way is auto-balancing bridged method with 4-terminal pair configuration (4TPC), where the gate of MOSFET is connected to the two low terminals of the impedance-meter and the substrate electrode to the two high terminals. All shielding skins of 4 cables were connected to each other near the probe needles. The second way is an I-V method where the substrate of measured device is grounded and the gate is connected to the signal terminals (IVGD). Cascade ACP high frequency probe (S-G) was connected to the impedance-meter with Agilent 42941A impedance-probe. Calibrations were executed for both configurations using an impedance standard substrate.

3. Results and Discussion
First, the limitation of 4TPC is discussed. Fig.1 shows ω-dependence of Im(Z) under the strong accumulation condition measured by 4TPC. In case of impedance measurements of ultra-thin gate insulators, many unexpected resonance structures appear above 1MHz. Therefore, measurements are limited only below 1MHz in 4TPC. As shown in Fig.2, in the low ω region, Im(Z) is proportional to ω at various Vg's and becomes positive or inductive under strong Vg's, which results in negative C. If the equivalent circuit model with a series inductor L (3ECM plus L) is the case, Im(Z) behaves in the low ω region as below:

\[ \text{Im}(Z) = \alpha \cdot (-CR_s^2 + L) \]  

(1),

where L is constant. Even if L was intrinsic property of the device [7], L might not depend strongly on Vg on the condition that electron current is much larger than hole current in p-well [8]. Therefore, the slope of Im(Z) increases monotonically to L as stronger Vg is applied. In Fig.3, the slopes of Im(Z) in Fig.2 vs. Vg are shown for the following two conditions: (a) the prober frame and the guard shield of the chuck where the Si wafer was put were grounded and (b) the guard was floated and the chuck grounded. Unexpectedly, Im(Z) appears on each condition and values of these peaks are different from each other, which indicate that the inductive behavior of Im(Z) relate mainly to capacitance between a wafer (or the chuck) and the ground. In Fig.4, we present another equivalent circuit model considering the whole measurement system. It contains the input resistance (Rσ=25Ω), a series inductor, and a stray capacitor (Cg) across the ground and the chuck. In this model, apparent Im(Z) behaves in low ω region as below:

\[ \text{Im}(Z) = \alpha \cdot (-CR_s^2 + C_gR_gR_s + C_gR_gR_s + L) + \alpha \cdot 0 \]  

(2),

where a term of \( \omega^2 \) is omitted. The peaks in Fig.3 originate from the first and second terms in the right side of Eq.2 because only Rσ depends strongly on Vg. The amplitude difference of these peaks corresponds to the different values of Cg on (a) and (b). When the third term dominates, Im(Z) is proportional to Rσ, which explains the substrate resistance dependence of positive inductance [7]. These behaviors are caused mainly by the signal returning through Cs. In Fig.5, CV curves calculated in terms of Eq.2 using the measured values of Cs, Rσ and Rc are shown. Here, Rs's are estimated from the DC Ig-Vg measurements. The curves calculated by Eq.2 are more plausible than the ones by 3ECM, which indicates Eq.2 describes the measurement system more accurately. However, the calculation is hard and large errors are unavoidable because Eq.2 contains many parameters which should be measured independently.

Next, the superiority of IVGD to 4TPC is demonstrated. In Fig.6, the trajectories of impedance of the same devices measured at a strong Vg by 4TPC and IVGD are shown. The curves of IVGD are much smoother semicircles, which is expected for 3ECM, than that of 4TPC in whole ω region (1kHz to 100MHz). This is because in IVGD, (1) there is no residual signal path in measurements in, (2) the signal peaks in between the amperemeter and the volt-meter, (2) the chuck can be grounded which can reduced the effects of stray capacitance, and (3) L and parasitic capacitance in IVGD is smaller than those in 4TCP, since the configuration of IVGD is simple. In 3ECM, the radius of semicircle corresponds to Rσ/2 and the center is on the coordinate of (Rσ/2+Rgσ, 0). Rσ and Rgσ can be extracted easier by the least square fit to the square of Im(Z) than direct fitting to Im(Z), which is the non-linear function of Re(Z). C can be calculated at any frequencies using Im(Z) and

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Re(Z) - R∞, where Re(Z) is the real part of impedance. Fig. 7 shows the normalized CV curves of MOSFET's. To subtract parasitic capacitance, the gate length dependence of C at Vg=0V of MOSFET's with the same gate width is used. In Fig.7, it is obvious that the curve measured by IVGD in parallel mode is degraded less than that by 4TPC in parallel mode. However, reduction of C in strong Vg due to R∞ is observed for IVGD in PM. This can be corrected by applying 3ECM to IVGD. It can be read that IVGD is superior to 4TPC and 3ECM is valid for IVGD. However, for thinner insulator measurement, other residual impedance elements which may exist in IVGD should be considered.

4. Summary
We clarified that in auto-balancing bridged method with 4-terminal pair configuration, a current flow along a stray capacitor across the well and the ground causes negative capacitance in case of impedance measurements of ultra-thin gate insulators. We proposed another method, which is an I-V measurement on MOSFET's whose substrates are grounded. According to its simple configuration, the measurement frequency was extended up to 100MHz and stray capacitance and residual path of the signal were eliminated. This greatly helps to realize accurate measurement of impedance and also increases the validity of applying the 3-element circuit model.

References