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Impact of Nitrogen Profile on Negative-Bias Temperature Instability and CMOS Performance

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Abstract

We have investigated an impact of nitrogen profile in SiON gate-dielectric on negative bias temperature instability (NBTI) and sub-100-nm CMOS device performance. The main component of the V_T shift caused by NBTI is found to be increased interface trapping, and interfacial nitrogen enhances the generation of interface traps. Suppressing the interfacial nitridation through radical nitridation improved the NBTI lifetime. CMOS circuits with a low-interfacial-nitrogen SiON gate-dielectric formed using N-radicals performed ($1/\tau_{PD}$) 10% better and were ten times as reliable.

Introduction

A low-leakage, highly reliable ultrathin SiON gate-dielectric is essential to achieve high-performance sub-100-nm CMOS devices [1]. SiON gate-dielectrics fabricated by various techniques have been reported [2]–[4]. However, nitrogen incorporation into an ultrathin gate oxide increases NBTI [5]. In this paper, we investigate nitridation process and an impact of nitrogen profile in SiON gate-dielectric on device properties and reliability, and discuss the NBTI mechanism.

Gate-dielectric fabrication

We fabricated ultrathin SiON films by using an electron-cyclotron resonance (ECR) plasma. Three processes of nitridation (A: N-radicals, B: N-radicals + N-ions, and C: N-radicals + O-radicals) were applied after 1.6-nm (A and B) or 1.2-nm (C) radical-base SiO_2 formation to control the nitrogen profiles. Figure 1 shows SIMS profiles of the nitrogen in the gate SiON fabricated under the three processes. The Si/SiON interface was located at 2.2 nm. Process "C" led to a broad nitrogen profile with a high nitrogen intensity at the interface. Process "A" formed a steep nitrogen profile with low nitrogen intensity at the interface. The interfacial nitrogen intensity obtained through process "B" was higher than that with process "A" because the N-ions used in process "B" correctly nitridate the interface.

Results and discussion

A) Gate-leakage current and drivability

Figure 2 shows the I_G-EOT (equivalent oxide thickness) characteristics of SiON films fabricated by process "A", "B", and "C". The nitrogen concentration measured by XPS (N_{XPS}) is also shown. Nitridation decreased the gate-leakage current for both the NFET (Fig. 2(a)) and the PFET (Fig. 2(b)). Figure 3 shows the N_{XPS} dependence on the $I_{ON}T_{OX\text{-}inv}$ (which is the drain current normalized by electrical oxide thickness) degradation from the SiO_2 in the PFET. As N_{XPS} increased, $I_{ON}T_{OX\text{-}inv}$ for all three processes deteriorated but the rate of deterioration was greater for process "B" than for process "A". If we compare SiON films with the same N_{XPS}, process "C" led to the worst films. These results indicate that $I_{ON}T_{OX\text{-}inv}$ of a PFET is sensitive to the interfacial nitrogen concentration and that interfacial nitrogen degrades the hole mobility. Process "A" suppressed the interfacial nitridation and can be used to control the degradation of PFET drivability.

B) Reliability (NBTI)

We measured the NBTI of PFETs with an S/D and an n-well electrode grounded at 400K. Figure 4 shows the I_D-V_G characteristics of a PFET, fabricated using process "C", before and after bias temperature (BT) stress. The BT stress caused a –28-mV V_T shift, a 1.8-mV/dec subthreshold-swing (S) increase, and a 4% Gm degradation. The V_T shift caused by the NBTI is the key to ultrathin SiON gate-dielectrics. It has been reported that the main component of the ΔV_T caused by NBTI is due to a fixed charge increase in the SiON, but ΔV_T was not separated into an interface trap component (ΔD_{it}) and a fixed charge component (ΔQ_{fix}) [5]. Figure 5 shows the stress-time dependence on total ΔV_T and separated ΔV_T. The total ΔV_T was separated into a ΔD_{it} component and a ΔQ_{fix} component using techniques based on subthreshold-current measurement [6]. These results indicate that the main component of ΔV_T is caused by an increase of D_{it} irrespective of the nitridation processes. To confirm the ΔV_T component, we also carried out C-V measurements. Figure 6 shows the C-V characteristics of a PMOS with SiON film (EOT ≅ 1.8 nm, formed by process "A") before and after BT stress. The C-V curves did not shift near V_{FB} (the flatband voltage V_G was ~0.9 V), but shifted in the negative direction in inversion. Figures 5 and 6 indicate that a large quantity of interface traps was generated by BT stress while there was only a slight increase in the fixed charges. Figure 7 shows the N_{XPS} dependence on the NBTI lifetime that fell as N_{XPS} increased. The NBTI lifetime for the SiON films with a low interfacial nitrogen concentration (formed by process "A") were improved by about 4 times of magnitude compared to that in films with a high interfacial nitrogen concentration (those formed by process "C") at the same N_{XPS}. Figure 8 shows a schematic of the NBTI mechanism for SiON. Interfacial nitrogen enhances the generation of interface traps during BT stress, but process "A" (with N-radicals) results in so low interfacial nitridation that suppresses the NBTI degradation.

C) CMOS performance and reliability

Figure 9 shows the total gate leakage (I_{GTOTAL}) versus the CMOS performance ($1/\tau_{PD}$) and the NBTI lifetime. τ_{PD} and I_{GTOTAL} were calculated as

$$\tau_{PD} = C_L V_{DD} (1/I_{ON(NMOS)} + 1/AI_{ON(PMOS)}),$$
$$I_{GTOTAL} = I_{G(NMOS)} + AI_{G(PMOS)},$$
$$A = I_{ON(NMOS)} / I_{ON(PMOS)} = \text{constant},$$

where C_L and V_{DD} are load capacitance and supply voltage, respectively.

We have demonstrated that process "A" improves performance ($1/\tau_{PD}$) by 10% and reliability by a factor of ten compared with process "C" at the same I_{GTOTAL} condition.

This result indicates that the steep nitridation profile with low interfacial nitrogen concentration that can be obtained by radical nitridation is important to fabricate a low gate-leakage, high-performance, and highly-reliable SiON gate-dielectric for CMOS devices.

Summary

We found that the main component of the V_T shift caused by NBTI is increased interface trap generation due to interfacial nitrogen. Nitridation using N-radicals, resulting in steep nitrogen profile with low interfacial nitridation, is an effective way to fabricate a low-leakage, high-performance SiON gate-dielectric that suppresses NBTI degradation in CMOS devices.

References

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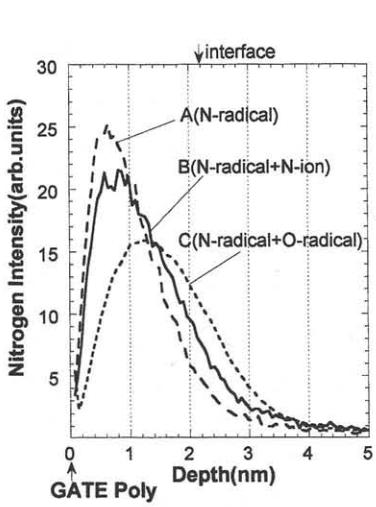


Fig. 1 SIMS profiles of the nitrogen in SiON fabricated by different processes. Process "A" can form steep nitrogen profile with low interfacial nitrogen intensity.(Interface:2.2nm)

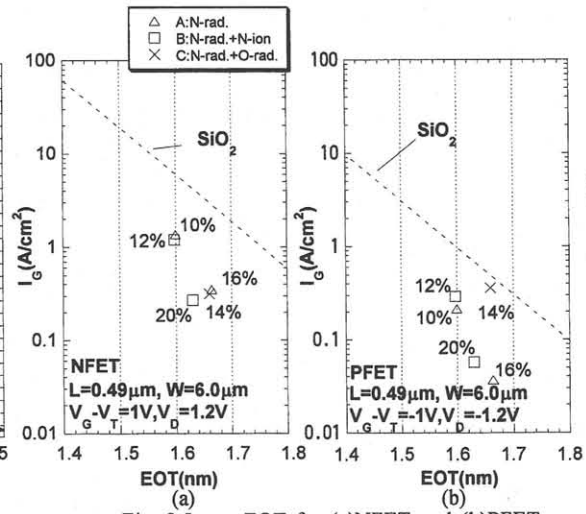


Fig. 2 I_G vs. EOT for (a)NFET and (b)PFET. Open triangles indicate process "A". Open squares indicate process "B". Cross mark indicates process "C". Nitrogen concentration estimated by XPS (N_{XPS}) are also indicated.

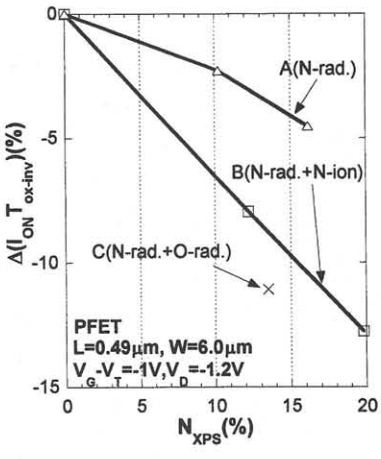


Fig. 3 N_{XPS} dependence of $\Delta(I_{ON}T_{OX\text{-}INV})$ degradation from radical SiO_2 in PFET. Process "C" (N-radicals and O-radicals) degrades $\Delta I_{ON}T_{OX\text{-}INV}$ much more than the others with the same N_{XPS}.

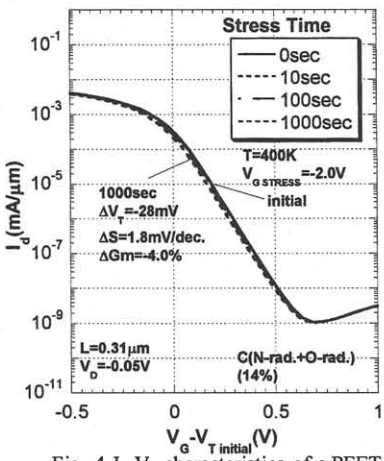


Fig. 4 I_d-V_g characteristics of a PFET before and after bias temperature (BT) stress. BT stress caused V_T shift, S increase, and Gm degradation.

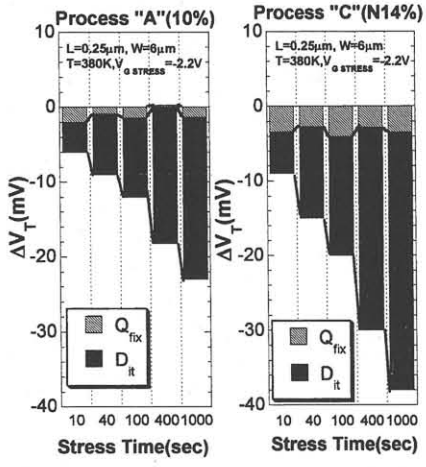


Fig. 5 BT stress time dependence of Total ΔV_T and separated ΔV_T. Total ΔV_T was separated into an interface trap components($\Delta V_T(D_{it})$) and a fixed charge components ($\Delta V_T(Q_{fix})$) using techniques based on subthreshold-current measurements[6]. $\Delta V_T(D_{it})$ is the main component of Total ΔV_T.

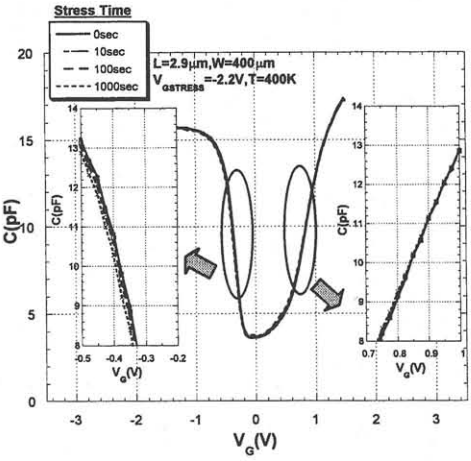


Fig. 6 C-V characteristics of SiON(EOT≅1.8nm) before and after BT stress. The SiON is fabricated by process "A" (N-radicals).

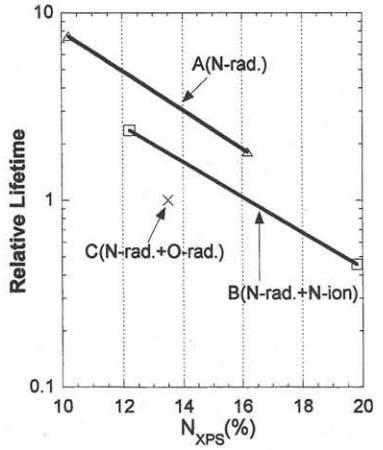


Fig. 7 N_{XPS} dependence of NBTI Lifetime. Process "C" (N-radicals and O-radicals) degrades lifetime much more than the others with same N_{XPS}.

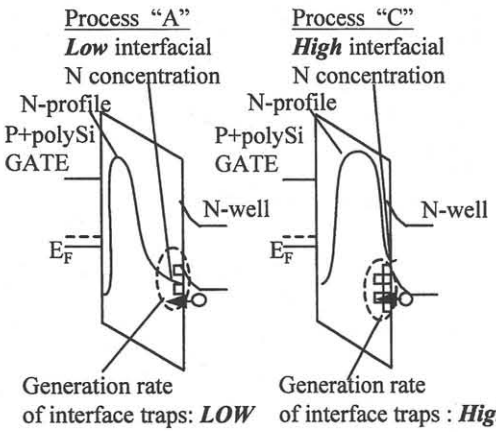
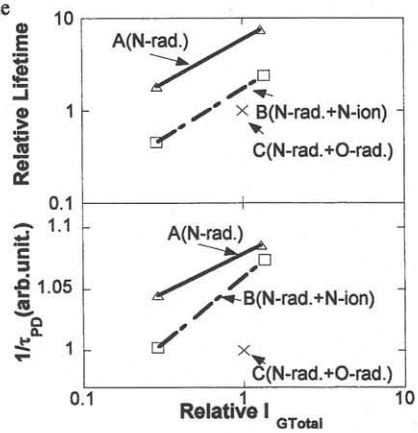


Fig. 8 Schematic of NBTI mechanism for SiON. Interfacial nitrogen enhances the generation of interface trap during BT stress. Process "A" results in low interfacial nitridation that suppresses NBTI degradation.



$\tau_{PD} = C_L V_{DD} (1/I_{ON(NMOS)} + 1/AI_{ON(PMOS)})$
$I_{GTOTAL} = I_{G(NMOS)} + A I_{G(PMOS)}$,
$A = I_{ON(NMOS)} / I_{ON(PMOS)}$ =constant
C_L:load capacitance, V_{DD}:supply voltage

Fig. 9 Relative I_{GTOTAL} vs. CMOS performance ($1/\tau_{PD}$) or relative lifetime. Process "A" is an effective way to fabricate a low-gate- leakage and high performance SiON that suppresses NBTI degradation in CMOS devices.