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Bias and Temperature Dependent Reliability Issues in a 0.18um Generation CMOS Multi-Oxide SoC Technology

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Abstract- System-on-a-chip (SoC) has received considerable attention in the modern and the future dual gate CMOS technology. The critical technological requirement of SoC is to integrate CORE and I/O circuits in one multi-function chip. However, with an ever increasing high density and power dissipation of SoC, it gives rise to an increase of the chip temperature. The negative bias temperature instability (NBTI), which arises at high temperature (high T) has also been shown to be the critical reliability issue, especially in pMOSFETs. In this study, a complete test of seven kinds of stress conditions, which will affect the device lifetime, will be investigated in the 0.18um generation SoC technology with a multiple oxide thickness and multiple applied biases. Therefore, we provide a guideline for the next generation SoC CMOS technology. In nMOSFET, the temperature effect is weak such that the conventional HC stress (i.e., $I_{B,max}$) at room temperature dominates device lifetime. While, in pMOSFET, temperature effect is critically important such that the NBTI-like HC stress determines device lifetime.

I. Device Preparation

The CMOS devices were fabricated by using 0.18um generation SoC technology. The core devices (L=0.18μm; t_{ox}=32Å) and I/O devices (L=0.35μm; t_{ox}=65Å) were designed and tested on the same chip. The applied voltages (stress biases) for the core and I/O devices in SoC application are 1.8V (2.5V) and 3.3V (4.5V), respectively. In order to obtain a high-quality and high-reliable gate oxide, the post-oxide N_2O annealing has been used. After these manufacturing processes, these devices were stressed with 7 different kinds of bias conditions for reliability tests.

II. Results and Discussion

A. Bias and Temperature Dependent CMOS Reliability

Positive Temperature Dependent Behavior: Figure 1 shows the bulk current as a function of temperature and drain/gate bias. At V_D=1.8V, the bulk current increases with increasing temperature; while at V_D=3.0V, it decreases with increasing temperature. Figure 2 shows the temperature and drain bias dependence of maximum bulk current. Positive temperature dependent bulk current occurs at low V_D bias, while negative temperature dependent behavior occurs at high V_D bias. When a device is stressed at low V_D bias of interest, its degradation is proportional to the temperature. Results show that pMOSFET seems to be more sensitive to the temperature effect.

Device Degradation for SoC devices: Figure 3 shows the drain current degradation for CMOS devices. It was shown that, in nMOSFET, the device reliability is less dependent on the temperature, while in pMOSFET, the V_G=V_D stress causes a largest degradation at room T (25°C). Figure 4 shows the pMOSFET stressed under various conditions at room T (25°C) and high T (125°C). At room T, device degradation is dominated by negative oxide traps at low V_G and by positive oxide traps at high V_G. Moreover, at high T, the I_D degradation is enhanced by the positive oxide traps only.

B. High Temperature Reliability of pMOSFET

Negative Bias and Temperature Instability (NBTI) [5-6]: Figure 5 shows the NBTI degradation for both 0.18um and 0.35um pMOSFET's. The NBTI induced degradation increases with a reducing channel length and increasing temperature. Fig. 6 shows the substrate hot hole (SHH) enhanced FN and NBTI degradation. At high T, the SHH becomes more active to enhance the device degradation.

V_G=V_D stress at High T (NBTI-like HC stress): For the pMOSFET device under V_G= V_D stress, it is the so-called NBTI-like HC stress. Figure 7 shows the NBTI-like HC degradation which increases with increasing bulk current and temperature. Figure 8 shows the ratio of reverse mode and forward mode threshold voltage (V_{TH}) shift, in which the drain-side damage dominates in the reverse mode while the source-side damage dominates in the forward mode. From the experimental results, it was shown that, at room T, merely the HC effect occurs at drain-side; while at high T, the NBTI occurs at the source-side, and the HC + NBTI occur at the drain-side, which causes the same order of damage on both source and drain sides.

Summary for pMOSFET stressed at high T: To explain the above observations, a schematic diagram of the generated damage for devices after NBTI stress and NBTI-like HC stress is illustrated in Fig. 9. For NBTI stress, Fig. 9(a), the damage region is uniformly distributed in the entire channel. Its degradation *increases* with a reducing channel length. However, for the NBTI-like HC stress, the damage region is non-uniform distributed in the channel. The degradation *decreases* with a reducing channel length. This implies that NBTI will become more pronounced in a small geometry device, which is an important factor for a reliable design of next generation devices.

C. Reliability Test Criteria for SoC Circuits

Fig. 10 summarizes the comparison of 7 stress conditions in both core (0.18μm) and I/O (0.35μm) devices. Temperature dependence is weak in nMOSFET, thus the conventional HC test [6] is sufficient for reliability test. Nevertheless, temperature effect is significant in pMOSFET, in particular in shorter channel devices. So, the NBTI and V_G= V_D stress at high T (NBTI-like HC test) becomes critical in pMOSFET. Note that the NBTI degradation is enhanced in shorter channel pMOFET, but it is not important in nMOSFET and long channel pMOSFET.

Finally, Table I shows the quantitative data for Fig. 10 and highlights the 1st and 2nd reliability impact factor for core and I/O devices. To establish a highly reliable SoC circuit, we need to use the test criteria by considering the HC effect in nMOSFET, and temperature effect in pMOSFET.

In summary, we provide a complete reliability guidelines in an SoC chip. Seven kinds of reliability tests for both core and I/O devices have been studied. In nMOSFET, the temperature effect is weak at any bias. As a consequence, the conventional HC (i.e., $I_{B,max}$ stress at room T (25°C)) dominates device lifetime. On the other hand, in pMOSFET, temperature effect is critically important for lifetime prediction. As a result, the NBTI-like HC stress determines device lifetime. This is a useful guideline for the reliability study in the current and next generation SoC CMOS technologies.

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References

[1] C. H. Lee et al., in *IEDM Tech. Dig.*, p. 491, 1999.
[2] H. Hwang et al., *IEEE IRPS.*, p. 48, 1995.
[3] C. Hu, et al., *IEEE T-ED.*, vol. 20, no. 1, p. 295, 1985.
[4] N. Kimizuka et al., in *Symp. on VLSI Tech.*, p. 73, 1999.
[5] P. Aminzadeh et al., in *Symp. on VLSI Tech.*, p. 178, 1998.
[6] N. Kimizuka et al., in *Symp. on VLSI Tech.*, p. 92, 2000.

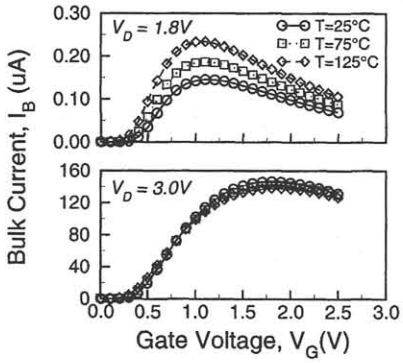


Fig. 1 Bulk current versus gate bias as a function of temperature for nMOSFET at different drain biases.

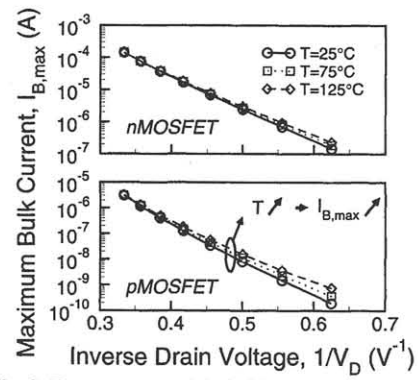


Fig. 2 Temperature and drain bias dependence of the maximum bulk current for both nMOSFET and pMOSFET devices.

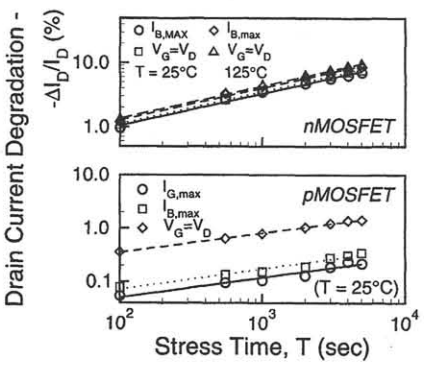


Fig. 3 Drain current degradations for CMOS devices under various stress bias conditions and temperatures.

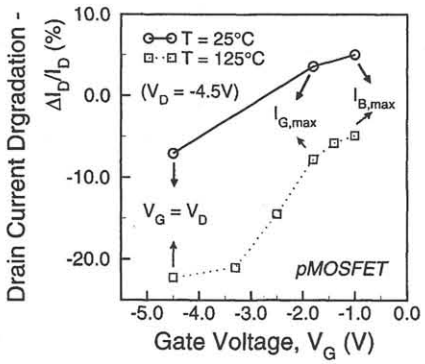


Fig. 4 Drain current degradation as a function of gate voltage at room temperature (25° C) and high temperature(125°C) for pMOSFET.

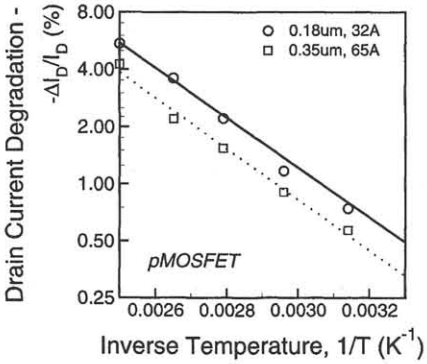


Fig. 5 Drain current degradations as a function of temperature for NBTI stress in pMOSFET.

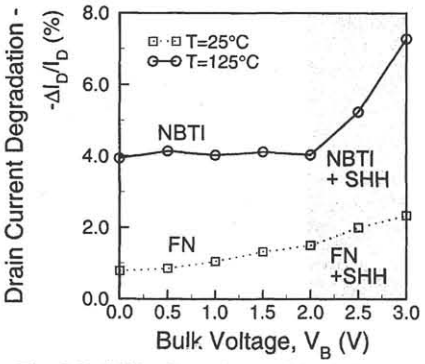


Fig. 6 Bulk bias dependence of the drain current degradation under NBTI and FN stresses in pMOSFET.

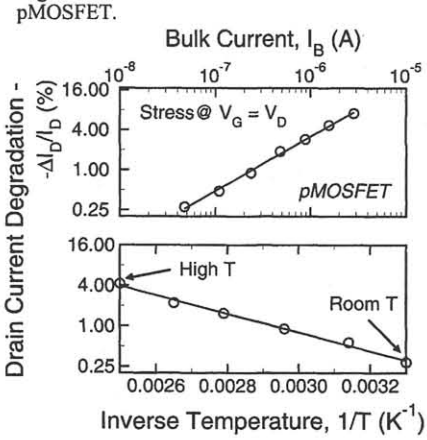


Fig. 7 *Upper-* The relationship between bulk current and drain current degradations. *Bottom-* Drain current degradation as a function of the temperature.

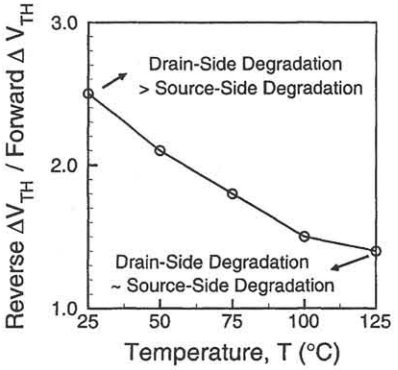
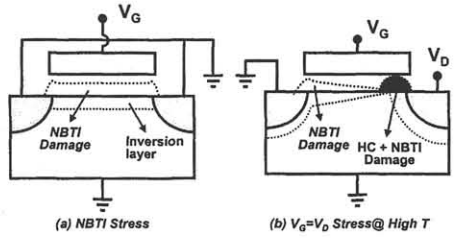


Fig. 8 Ratio of the reverse mode and forward mode V_{TH} shift under V_G=V_D stress at various temperatures.



	Distribution	Characteristics
NBTI	Uniformity	Temperature ↑ → Degradation ↑ Channel Length ↓ → Degradation ↑
V_G=V_D @ high T	Non-uniformity	Temperature ↑ → Degradation ↑ Channel Length ↓ → Degradation ↓

Fig. 9 An illustration for the comparison of the damage region in a pMOSFET under (a) NBTI stress and (b) V_G=V_D stress at high T.

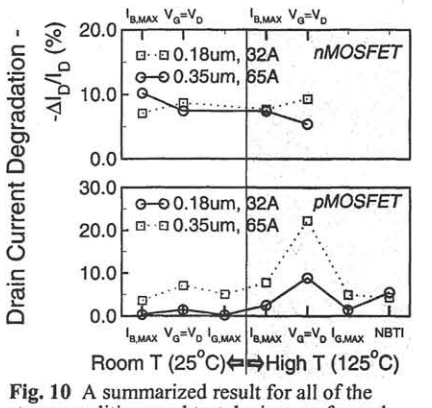


Fig. 10 A summarized result for all of the stress conditions and test devices performed in this work.

Drain Current Degradation (%)		nMOSFET 0.35um	nMOSFET 0.18um	pMOSFET 0.35um	pMOSFET 0.18um
Room T (25°C)	$I_{B,max}$	**10.2**	7.07	3.59	0.35
	$I_{G,max}$			5.04	0.22
	V_G = V_D	**7.43**	**8.66**	7.07	1.42
High T (125°C)	$I_{B,max}$	7.42	7.69	**7.80**	2.50
	$I_{G,max}$			4.90	1.40
	V_G = V_D	5.41	**9.30**	**22.3**	**8.90**
	NBTI			4.25	**5.47**

Table I (a) Drain current degradation for 0.35 and 0.18um CMOS devices under 7 different stress biases.

Reliability Issue	nMOSFET 0.35um	nMOSFET 0.18um	pMOSFET 0.35um	pMOSFET 0.18um
1st	$I_{B,max}$ @25°C	V_G = V_D @125°C	V_G = V_D @125°C	V_G = V_D @125°C
2nd	V_G = V_D @25°C	V_G = V_D @25°C	$I_{B,max}$ @125°C	NBTI @125°C

Table I (b) 1st and 2nd reliability impact factor for 0.35 and 0.18um CMOS devices.