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0.1 μm pMOSFETs with SiGe-Channel and B-Doped SiGe Source/Drain Layers

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1. Introduction

In order to realize the optimized MOSFET structure with sub-0.1 μm gate length, a super self-aligned ultrashallow junction formation technique instead of the conventional ion implantation method is essential. In the devices fabricated with such a new technique, the precise diffusion control of dopant is extremely important because the source/drain punch-through, which is an especially crucial problem for those devices, should be suppressed [1-2]. Moreover, the improvement of the effective carrier mobility in the channel region is also indispensable.

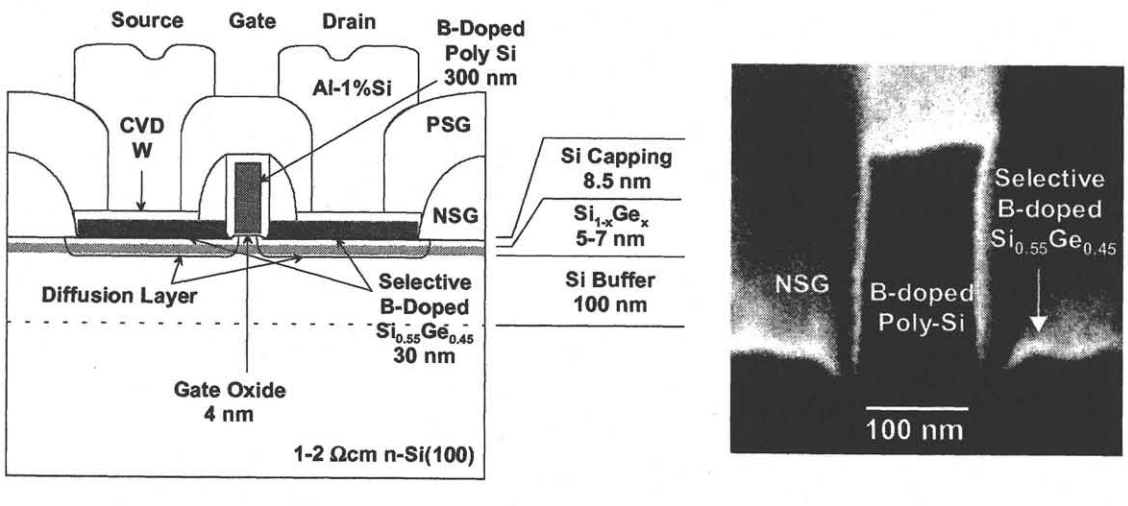
In this study, the fabrication of 0.1 μm $Si_{1-x}Ge_x$-channel (x=0-0.5) pMOSFET with ultrashallow junction source/drain formed by selective in-situ B-doped $Si_{0.55}Ge_{0.45}$ chemical vapor deposition (CVD) has been investigated.

2. Fabrication process

The schematic device structure and the cross-sectional SEM micrograph of the 0.12 μm $Si_{0.5}Ge_{0.5}$-channel S^3EMOSFET are shown in Fig. 1. At first, high quality 10 nm-thick Si/ 5-7 nm-thick $Si_{1-x}Ge_x$ (x=0-0.5)/ 100 nm-thick Si heterostructure was epitaxially grown on 1-2 Ωcm n-type Si(100) surface in a SiH_4-GeH_4-H_2 gas mixture using an ultraclean hot-wall low-pressure CVD (LPCVD) system, which was made ultrahigh vacuum compatible with gate valves and a turbo-molecular pump system [3-4]. A field oxide was formed on the heterostructure at 400°C by CVD and a 4 nm-thick gate oxide was grown by wet oxidation at 700°C. Then, 300 nm-thick in-situ B-doped poly Si as a gate was deposited in a Si_2H_6-B_2H_6-H_2 gas mixture by LPCVD at 550°C followed by thermal wet oxidation to form an etching mask. The mask was patterned by photolithography using a stepper and the gate length reduction was done by resist-ashing with oxygen plasma. After the oxide pattern formation by wet etching, the poly Si was etched using highly selective electron-cyclotron-resonance chlorine plasma [5]. Oxidation of gate and S/D surfaces and Si-nitride deposition by CVD were performed at 700°C, followed by dry etching to form nitride sidewall, which is a protective film for the sidewall oxide. After removing the oxide on S/D regions and the nitride on gate sidewalls, the in-situ B-doped $Si_{0.55}Ge_{0.45}$ was selectively and epitaxially grown on the S/D regions in a SiH_4-GeH_4-B_2H_6-H_2 gas mixture at 550°C by LPCVD [6-7]. Covering with CVD SiO_2, the B diffusion from the B-doped $Si_{0.55}Ge_{0.45}$ into Si was performed at 750°C for 3 hours. After the CVD SiO_2 sidewall formation by dry etching, tungsten was selectively deposited on the B-doped $Si_{0.55}Ge_{0.45}$ surfaces by CVD in order to reduce the parasitic resistance [1-2].

3. Results and discussion

Typical drain-current-voltage of a $Si_{0.5}Ge_{0.5}$-channel pMOSFET with a gate length of 0.12 μm is shown in Fig. 2. The maximum saturation drain current (I_D) is estimated as



a) b)

Fig. 1. a) Schematic diagram of $Si_{1-x}Ge_x$-channel super self-aligned ultrashallow junction electrode pMOSFET (S^3EMOSFET) and b) the cross-sectional SEM micrograph of 0.12 μm $Si_{0.5}Ge_{0.5}$-channel S^3EMOSFET

about 620 μA/μm at the gate voltage (V_G) = the drain voltage (V_D) = -2 V. The subthreshold slope was evaluated as 89 and 130 mV/decade at V_D = -50 mV and -1.5 V, respectively. The subthreshold slope of the $Si_{0.5}Ge_{0.5}$-channel devices with longer gate lengths than 0.12 μm, for example 0.16 μm, is smaller than 77 mV/decade even at V_D= -1.5 V. The drain current drivability of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs with Ge fraction of 0.4 or 0.5 and with gate length of 0.51 or 0.46 μm, respectively, is significantly improved by a factor of about 30%, compared with the conventional Si-channel device with a 0.51 μm gate length, and their maximum linear transconductance at V_D = -50 mV is enhanced by about 65%. It suggests that the effective mobility of holes in the $Si_{1-x}Ge_x$-channel significantly increases compared with that in the surface-Si-channel as reported earlier [4-5,8].

The dependences of threshold voltage (V_T) on gate length

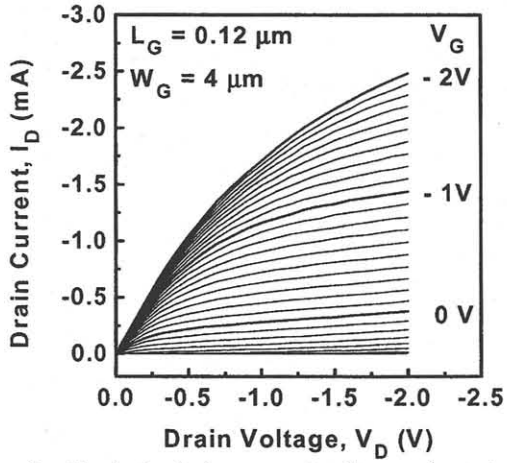


Fig. 2. Typical drain-current-voltage characteristics of 0.12-μm $Si_{0.5}Ge_{0.5}$-channel S^3EMOSFET.

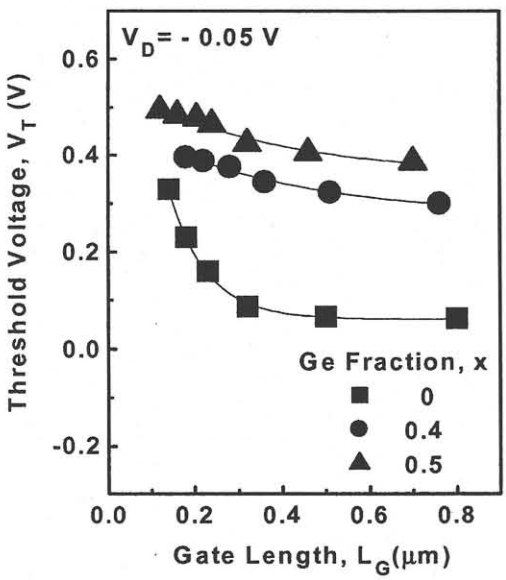


Fig. 3. Dependences of the threshold voltage when V_D = -50 mV on the gate length of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs.

of the $Si_{1-x}Ge_x$-channel S^3EMOSFETs are shown in Fig. 3 with Ge fraction as a parameter. The change of V_T with increasing Ge fraction of $Si_{1-x}Ge_x$ channel is resulted from the valence band shift in the $Si_{1-x}Ge_x$ channel. It is also found from the figure that the roll-off characteristics are improved for the $Si_{1-x}Ge_x$-channel MOSFETs, compared with the conventional Si-channel MOSFETs. This result indicate that, although the $Si_{1-x}Ge_x$-channel MOSFET is a buried-channel type, the short channel effect in the $Si_{1-x}Ge_x$-channel S^3EMOSFETs is well suppressed compared to the surface-channel type of Si-channel devices. This is due to the ultrashallow junction depth, estimated as approximately 20 nm, i.e., slightly below the $Si_{1-x}Ge_x$/buffer Si interface, and the suppression of the drain and source depletion-layer widths into the SiGe channel resulting from the reduction of the energy band gap by introducing Ge.

4. Conclusion

We have successfully fabricated 0.1 μm $Si_{1-x}Ge_x$-channel pMOSFETs with super self-aligned ultrashallow junction source/drain, formed by the selective in-situ B-doped $Si_{0.55}Ge_{0.45}$ epitaxy on source/drain by CVD and subsequent diffusion. The $Si_{1-x}Ge_x$-channel S^3EMOSFETs with x = 0.4-0.5 show higher performance than the Si-channel devices. Despite the buried-channel type, the short channel effect is suppressed in the $Si_{1-x}Ge_x$-channel devices, compared with conventional surface-channel Si MOSFETs due to the ultrashallow junction depth and the suppression of the drain and source depletion-layer widths resulted from the narrow band gap of $Si_{1-x}Ge_x$.

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