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Electrical Properties of High-k MIM Interlevel Capacitors Prepared for RF-CMOS Device Applications

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1. Introduction

Rapid growth in personal wireless communications gave significant importance on the accompanying high-frequency device technologies. For these devices, it is of great importance to fabricate high quality passive elements with low parasitic components, to ensure the high frequency operation. For this purpose, a metal/insulator/metal (MIM) capacitor prepared at an upper interlevel layer has been developed and investigated [1]. With a conventional SiO_2 or SiN dielectric of low capacitance density, the MIM capacitors still occupy large area that makes difficult to further increase circuit density and reduce the cost. To overcome this deficiency, it is considered to be promising to apply high-k material, like $SrTiO_3$ (ST) or $(Ba,Sr)TiO_3$ (BST) [2,3] as a dielectric. However, there are few reports on the high-k MIM capacitors prepared with the process temperature below 400°C, that is the maximum allowable temperature of the metallization process.

In this paper, we fabricated high-k MIM interlevel capacitors using ST or BST dielectric prepared by process conditions below 400°C, and investigated the basic and RF electrical properties of the capacitors, focusing on differences in the dielectric property between ST and BST films.

2. Experiment

Fig. 1 shows a schematic and cross-sectional SEM images of the MIM capacitor. A 200-nm-thick Pt bottom electrode, with a 50-nm-thick TiN underlayer, was deposited on silicon substrate with 800-nm-thick SiO_2. Then, ST or BST film was deposited by RF magnetron sputtering at 300°C, 0.1-0.2 Pa with Ar/N_2O gas, followed by a 60-nm-thick top Pt electrode deposition. Table I shows deposition conditions of the ST and BST films. The film thickness was set to be 70 nm, which gave good insulating property. Dry etching was done by RIE with O_2/Cl_2 gas. Post annealing was also done several times below 400°C to remove etching damages. Then a 400-nm-thick SiO_2 was deposited by plasma CVD with a thin adhesive layer. Finally aluminum interconnects to the top and bottom electrodes were fabricated with a TiN barrier metal layer via ~2 μm through-holes. Various capacitors of a wide variety of sizes and shapes were fabricated and measured by HP4155A, HP4194A for basic electrical properties and an HP8150C network analyzer for RF properties, respectively.

3. Results and Discussions

Figs. 2 and 3 show the relationship between capacitance or capacitance-density and the top electrode size, measured at 100 kHz, respectively. Dielectric constant and the capacitance density at zero-bias voltage were found to be k~70, ~9 fF/μm^2 for ST (almost flat for the capacitors from 25 μm^2 to 6400 μm^2 in size). The ST film consisted of fine polycrystalline grains and the dielectric constant was smaller than those of high temperature-grown films (k~200) [2, 3]; nevertheless, the capacitance density was very high in comparison with those of the conventional SiO_2 capacitor (~1 fF/μm^2). In contrast, BST showed even higher dielectric constant (k~140) and capacitance density ~ 19 fF/μm^2, which decreased with increasing the top electrode size. Fig. 4 shows the capacitance-voltage relationship for 20x20-μm^2 size capacitor, revealing BST had relatively large voltage coefficient of ~7 %/V at 3V, while ST had ~3 %/V. Fig. 5 is leakage current density-voltage curve of the capacitors showing that BST had a larger leakage than ST. From the data in the Figs. 4 and 5, leakage/capacitance values were found to be still under 1 fA/fF at 3V for both films.

From these results, it is concluded that both ST and BST films have high dielectric constant, capacitance density and low leakage despite the low process temperature below 400°C. However BST has a disadvantage of large voltage coefficient, in addition, the non-linearity in capacitance as a function of the size (possibly due to stress-induced effect [4]). Hence, ST is considered to be more appropriate for circuit design with good capacitance density and moderate voltage coefficient.

RF properties of the MIM capacitors were evaluated by measuring S-parameters of the 1-port type test pattern (as shown in Fig. 6) from 0.1 to 15 GHz. The S-parameters of a dummy pattern without a capacitor cell were also measured to calculate the intrinsic S-parameters. Fig. 7 shows the lumped equivalent circuit model for the present MIM capacitors and a formula for the complex impedance (Z) of the circuit, where an intrinsic capacitance (Cs), a series resistance (Rs) and an inductance (Ls) were considered. Fig. 8 is the RF response of the MIM capacitors with a square top electrode of 5x5 μm^2. The imaginary part ($-1/\omega Im[Z]$) of the impedance showed only a slight decrease, revealing both the ST and BST maintain their dielectric properties up to GHz range. (The increase at ~10 GHz for BST was caused by resonance effect of the circuit.) Table II shows the fitted parameters of the lumped equivalent elements for 15x15 μm^2 cell capacitors, revealing that, by using ST or BST, it is possible to fabricate the MIM capacitors of practical capacitance (2 ~ 5 pF) in the small size with very low Rs (~1.3 Ω) and Ls (~0.05 nH), applicable to GHz range operations.

4. Conclusions

We have successfully fabricated high-k MIM interlevel capacitors using $SrTiO_3$ or $(Ba,Sr)TiO_3$ by conventional processes below 400°C, with high capacitance densities of ~9 fF/μm^2 for ST, and ~19 fF/μm^2 for BST. ST is considered to be more suitable than BST for the smaller voltage coefficient and good linearity in the capacitance-size relationship. The measurements of the RF properties using 1-port type test patterns have revealed that the high-k MIM capacitors maintain their capacitance up to ~ 10 GHz, with low serial resistance and inductance. The high-k MIM interlevel capacitor technology is promising for future RF-CMOS devices applications.

Acknowledgments

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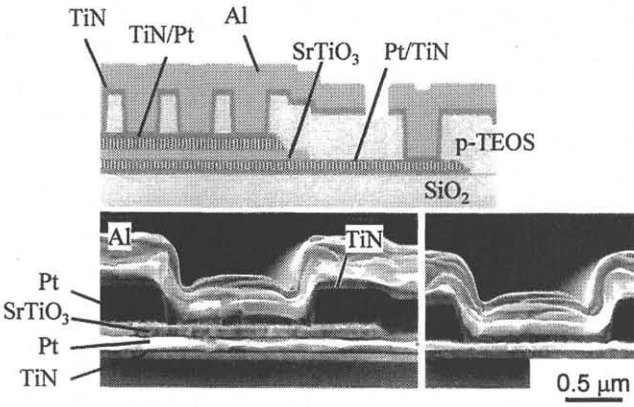


Fig. 1 Cross-sectional structure of MIM capacitor.

Table I Deposition conditions for ST and BST films.

Substrate temperature	300 °C
Method	RF magnetron sputtering
RF-power	850 W
Gas	Ar / N_2O (4:1)
Pressure	0.1 ~ 0.2 Pa
Deposition time	35 min
Film thickness	70 nm

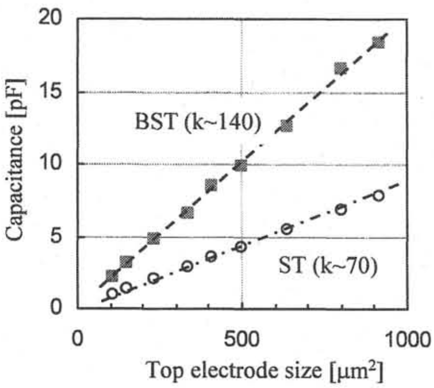


Fig. 2 Capacitance-Size relationship.

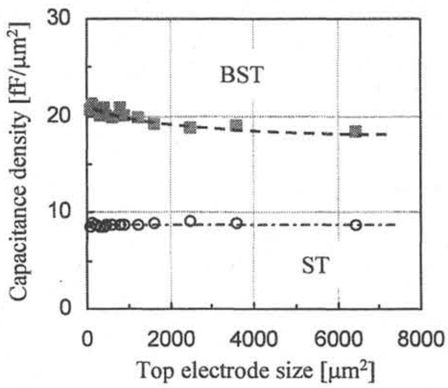


Fig. 3 Capacitance density-Size relationship.

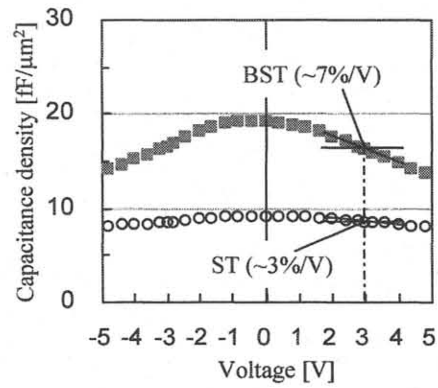


Fig. 4 Capacitance density-Voltage relationship. (20x20-μm² cell)

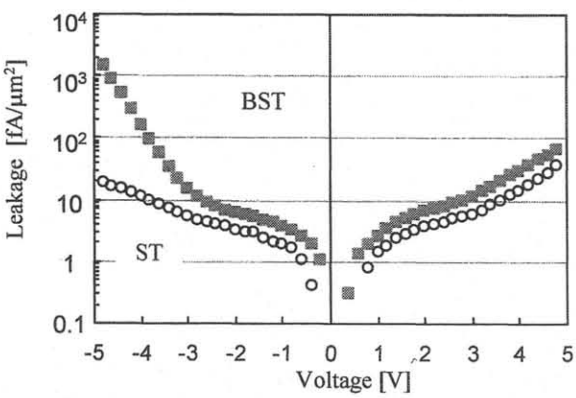


Fig. 5 Leakage-Voltage characteristics of the MIM capacitors (100 integrated cells of 20x20-μm² in size.)

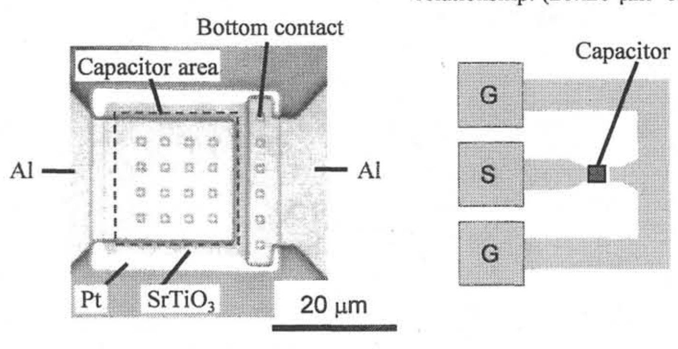
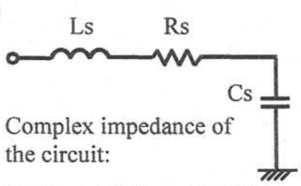


Fig. 6 Optical micrograph and schematic of 1-port type test pattern.



Complex impedance of the circuit:

$Z = Rs + i\,(\omega Ls - 1/\omega Cs)$

Fig. 7 Lumped equivalent circuit of the MIM capacitor used for parameter fitting.
Cs; intrinsic capacitance,
Rs; series resistance,
Ls; serial inductance

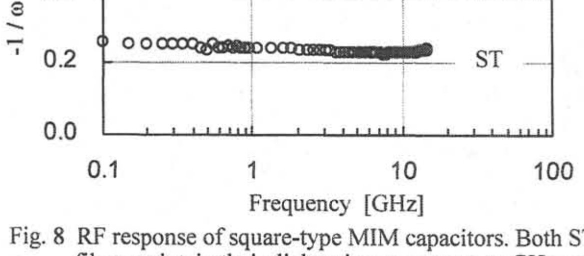


Fig. 8 RF response of square-type MIM capacitors. Both ST and BST films maintain their dielectric property up to GHz range.

Table II Fitted parameters of MIM 15x15 μm² size capacitors from S-parameters measured at 0.1 - 15 GHz.

Values	ST	BST
Cs	1.8 pF	4.3 pF
Rs	1.3 Ω	1.2 Ω
Ls	0.05 nH	0.05 nH