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Non-monotonous Transition of SOI History Effect from FD to PD Modes

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1. Introduction

With low parasitic capacitance and low back-bias effect, SOI devices are promising for high-speed and/or low-power applications. They can be classified as fully-depleted (FD) or partially-depleted (PD), depending on the condition of the body. The choice between these two types is important and can be critical in determining circuit performance.

One of the big differences between these two types is the history effect. With higher body-carrier density, PD devices are more susceptible to the fluctuation of body charge than FD devices. Many reports, such as [1-3], have characterized the history effect in FD and PD devices; however, its transition between FD and PD modes is not discussed experimentally.

To clarify the border between them, we experimentally investigated the history effect in FD and PD devices with various top silicon layer thickness and precisely analyzed its behavior using 2D process- and device-simulators.

2. Devices and Simulators

The devices were prepared using 0.13μm SOI CMOS technology similar to that in [4]. A TEM image of the device structure is shown in Fig. 1 and its design parameters are listed in Table. 1. The gate length is 130 nm and the top silicon layer thickness, T_{si}, on buried oxide varies from 25 nm to 60 nm. The process conditions, except for T_{si}, were kept constant for all devices. The actual T_{si} in each die was measured and determined using the CV method [5]. In Fig. 2, the measured T_{si} is compared with that estimated from initial wafer and process conditions. The good slope-of-one relation between them means good accuracy of obtained T_{si}.

Figure 3 plots threshold voltage against T_{si}. The slope of the V_{th}-T_{si} curve is relatively steep for thinner T_{si} (FD region), then, it flattens out at thicker T_{si} (PD region). The simulation results (plotted as lines) agree well with the measurements. To accurately simulate our devices, the process and device simulators, T-SUPREM4 and MEDICI respectively, were used. The simulation also agrees well with the measured I_d-V_g characteristics (Fig. 4).

3. History Effect – Results and Discussion

A. Experimental results

The experimental measurements of the history effect on switching speed of a 294-stage inverter chain are shown in Fig. 5. The propagation delays in response to the 1st and 2nd edges of a 4ns pulse, measured using the setup shown in Fig. 6, are shown as a function of pulse period. In shorter pulse period, especially near the pulse duty ratio of 50%, the 1st and 2nd switching delays are the same as that of the ring oscillator. This is, so-called, the steady state. As the pulse becomes longer, the 1st and 2nd switching delays become different. This difference is due to the history effect.

The history effect, defined as the difference between the 1st and 2nd switching delays at the pulse period of 1 msec., is shown in Fig. 7 as a function of T_{si}. It clearly has a peak of around 20% at T_{si} of around 35 nm. Circuit analysis using MEDICI (as schematically shown in Fig. 8) also indicates a peak at similar T_{si}, as shown in Fig. 7.

B. Analysis using 2D simulators

To investigate the peak of the history effect, the body charge was analyzed using the simulators. Since the history effect is understood as the difference in the body charge at different switching conditions, so that, the body accumulated carriers were calculated. Figure 9 shows the maximum hole concentrations in the NMOS body, N_{acc-1} and N_{acc-2}, at the moments just prior to the 1st and 2nd fall-time switching. The moments are also indicated as the dots shown in Fig. 10, which schematically explains the node voltages and the body couplings before and after the switching.

N_{acc-1} is determined by the DC-coupling balance between the inflow such as impact ionization and reversed diode currents and the outflow through forwarded diode current, as shown in Fig. 10. N_{acc-1} in thinner T_{si} devices is quite low because the potential barrier for holes in source-body diode is low and N_{acc-1} becomes high as T_{si} increases. On the other hand, N_{acc-2} is determined by the AC-coupling at previous switching (rise-time switching). N_{acc-2} in thinner T_{si} devices is negligible because of a lack of body-to-drain capacitance and N_{acc-2} becomes high as T_{si} increases with strong capacitive couplings. As a result, the difference between N_{acc-1} and N_{acc-2}, which is also shown in Fig. 9, has a peak. This peak is the cause of the non-monotonous transition of the history effect shown in Fig. 7. Body-to-drain capacitance was also calculated and Fig. 11. shows that thicker T_{si} devices have enough capacitance to increase N_{acc-2} in Fig. 9 through the capacitive coupling at output-rise switching.

As shown in Fig. 7, there are two ways to suppress the history effect, that is, designing appropriate T_{si} in FD/NFD (Nearly Fully-Depleted) or PD device regions, which are on thinner or thicker side of the peak. Since the junction capacitance is present in PD devices and absent in FD/NFD devices, FD/NFD device region will be preferable for ultra low-power applications with less parasitic capacitances.

4. Conclusion

The transition of the history effect from FD to PD modes was experimentally evaluated. It was found that the history effect has a peak around the boundary of the PD and FD/NFD operating modes and this behavior can be well explained by the coupling model of body charge.

References

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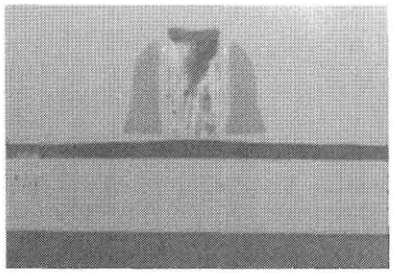

Fig. 1 Cross-sectional TEM image

Table. 1 Device design parameters

Gate Poly Si Thickness	150 nm
Gate SiON Thickness	1.8 nm
Top Si Thickness	25~60 nm
Buried Oxide Thickness	100 nm
Gate Length	130 nm
Co Sputter Thickness	5 nm

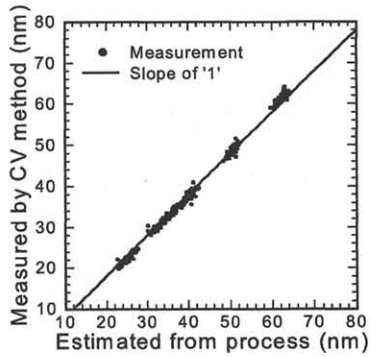

Fig. 2 Top Si layer thickness, Tsi

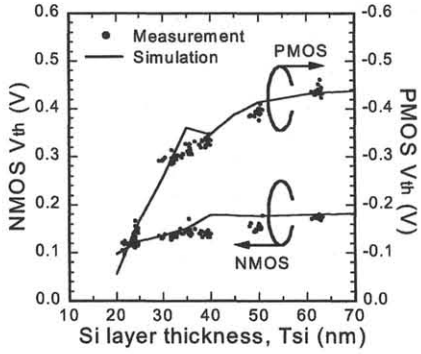

Fig. 3 Threshold voltage at Vds=±1.2 V.

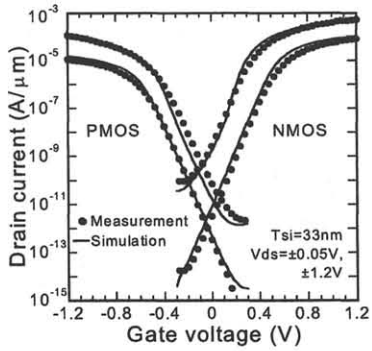

Fig. 4 Id-Vg characteristics at Tsi=33 nm.

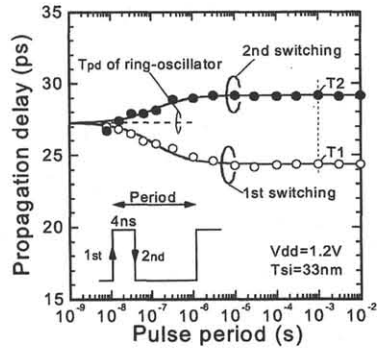

Fig. 5 Switching-delay variation

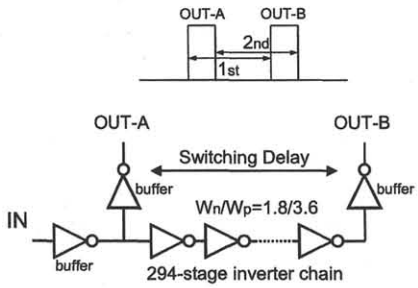

Fig. 6 Switching-delay measurement setup

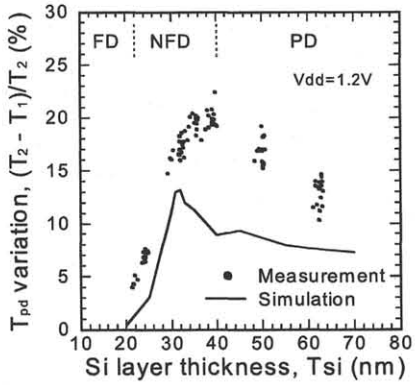

Fig. 7 Pulse stretch due to the history effect

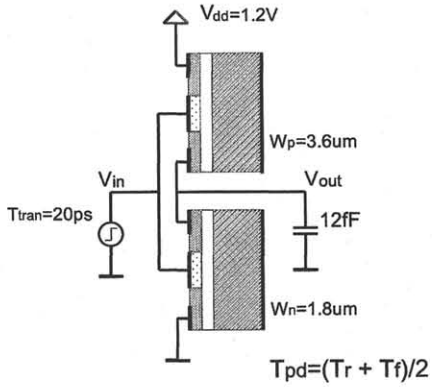

Fig. 8 Circuit analysis (MEDICI)

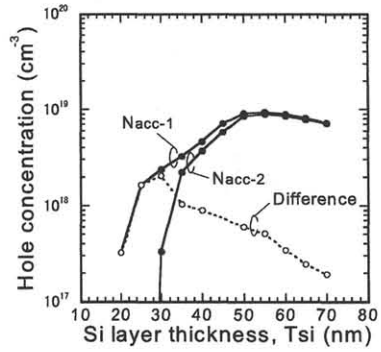

Fig. 9 Accumulated body holes just prior to the switching

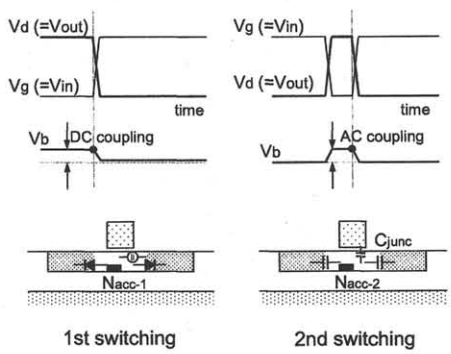

Fig. 10 Behavior during switching. Node voltages (top) and couplings (bottom).

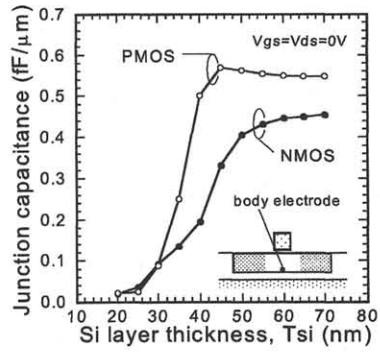

Fig. 11 Capacitance between drain and very small body electrodes