Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 74–75

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Elevated Source/Drain Engineering with 0.22-nm-Rms Smooth Surface Morphology for 90-nm-node Ultrathin-SOI CMOS

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1. Introduction

Reduction of the SOI thickness (T_{SOI}) in SOI CMOS devices is required not only to realize fully-depleted FETs but also to improve the performance of partially-depleted (PD) FETs through reduced source/drain (S/D) sidewall junction capacitance (C_{jswg}) and suppression of the floating-body effect [1]. On the other hand, aggressive T_{SOI} reduction increases the parasitic S/D series resistance (R_{sd}) [2]. To solve this problem, the elevated S/D structure has been strongly required for high performance ultrathin SOI CMOS [2]. As the most promising process to realize the structure, selective epitaxial growth (SEG) has been extensively studied [3]. In this paper, we point out, for the first time, the importance of the surface morphology of the epitaxial Si layer (epi-Si) in elevated S/D ultrathin SOI CMOS devices. We experimentally demonstrate a novel SEG technology that provides extremely smooth epi-Si surface on SOI and then discuss the impact of the epi-Si surface morphology on 90-nm-node ultrathin SOI FETs. Finally, the performance and yield of the fabricated FETs are shown.

2. Experimental

Elevated S/D 38-nm-thick SOI (*thin-SOI*) N/PFETs were fabricated. After the formation of full dielectric isolation and channel implantation, a 2.0-nm-thick gate oxide was grown. After the poly-Si gate electrode patterning, extension and pocket implantation were carried out. Gate sidewall spacers were then formed with Si_3N_4/TEOS, and epi-Si was selectively grown on the S/D regions by UHV-CVD with Si_2H_6 and Cl_2 gases. After deep S/D regions were formed, the gate and S/D were silicided by a conventional Co salicide technology. For comparison, elevated S/D bulk and 100-nm-thick SOI (*thick-SOI*) FETs were also fabricated.

3. Results and Discussion

Figure 1 schematically represents the degradation of the epi-Si surface morphology. Since the silicide layer inherits the morphology of the epi-Si, the silicide layer may come into contact with the BOX layer within any pits that are formed. A concern is that degradation of the epi-Si morphology will significantly modulate R_{sd} in an uncontrolled way because pits are formed randomly. Therefore, excellent epi-Si surface morphology is more critical in elevated S/D thin-SOI FETs than in bulk counterparts.

It has been reported that SiC islands formed on a Si surface during the sidewall etch-back degrade the surface morphology of epi-Si [3]. In this study, we investigated change of the epi-Si morphology by using no fluorocarbon gas in the sidewall etching . Figure 2 shows the dependence of average surface roughness (Ra) on the amount of overetching. Cl_2-plasma sidewall etching led to significantly lower roughness values and variation than was observed with CHF_3/Ar-plasma etching, which means Cl_2-plasma etching provides a wider process window. Figure 3 is a bird's-view SEM image of a PFET formed by CHF_3/Ar-plasma etching. Our SIMS results in Table I show that the Cl_2 plasma offered much lower coverage of C at the epi-Si/sub-Si interface than the CHF_3/Ar plasma. Therefore, the Cl_2-plasma etching does not form SiC islands, resulting in excellent epi-Si surface morphology.

Figure 4 is a bird's-view SEM image of the fabricated *thin-SOI* NFET with epi-Si thickness (H_{epi}) of 38 nm. The epi-Si was grown for 3.5 min at 680°C after preheating for 3 min at 850°C. Excellent surface morphology (0.22-nm rms) was apparent, as was reduced facet configuration. The H_{epi} deviation was below ±5% (Fig.5), and the smooth epi-Si enabled a uniform $CoSi_2$ film in the elevated S/D regions (Fig.6). Furthermore, Figure 7 shows the standard deviation of R_{sd} for the bulk, *thick-SOI* and *thin-SOI* NFETs. The R_{sd} deviation for *thin-SOI* devices was as low as that of the bulk and *thick-SOI* devices because of the good surface morphology. These results imply that UHV-CVD SEG combined with Cl_2-plasma sidewall etch-back is suitable for elevated S/D formation.

Figure 8 shows the short-channel characteristics of *thin-SOI* N/PFETs. The short-channel effect was suppressed to 80 nm. Figure 9 shows the $I_{on} - I_{off}$ characteristics of *thin-SOI* N/PFETs at $|V_d| = 1.2$ V. I_{on} was 720 and 290 μA/μm at $I_{off} = 10$ nA/μm for NFETs and PFETs, respectively. As shown in Fig.10, total junction capacitance of *thin-SOI* NFET was lower than that of the *thick-SOI*, and it was much lower than that of the bulk. This is because T_{SOI} scaling reduced C_{jswg} and the bulk had excessive S/D bottom junction capacitance. Additionally, f_{max} of the *thin-SOI* NFET at $L_{poly} = 100$ nm was 86 GHz. f_{max} is very important for high frequency operation [4]. Gate/Drain bridging is another important concern in elevated S/D engineering as illustrated in Fig.1. As shown in Fig.11, the high selectivity ensured that no gate/drain bridging was pronounced. It should be also noted that any other leakage phenomena were not observed.

4. Summary

We experimentally demonstrated a novel SEG technology which combines UHV-CVD and low-damage sidewall etch-back with Cl_2-plasma for elevated S/D ultrathin SOI CMOS devices. We found that the R_{sd} deviation of elevated S/D sub-40-nm-thick SOI FETs can be as low as that of bulk FETs because the excellent epi-Si surface morphology enabled a uniform $CoSi_2$ film. Moreover, neither gate/drain bridging nor any other leakage phenomena were pronounced. These results mean that this SEG technology is promising for elevated S/D ultrathin SOI CMOS devices for 90-nm technology node and beyond.

Acknowledgments

The authors would like to thank H. Maeda, K. Kuroda and Y. Wada for the AFM measurements, and H. Naruoka for the TEM observation.

References

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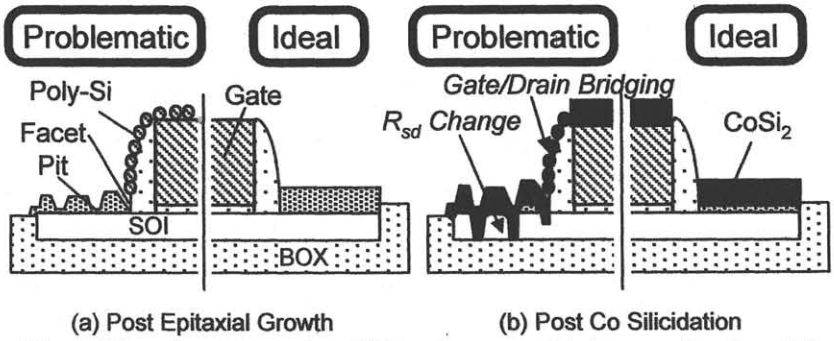

Fig. 1. Schematic representation of S/D resistance modulation caused by degraded surface morphology: structures after (a) epitaxial growth and (b) Co silicidation.

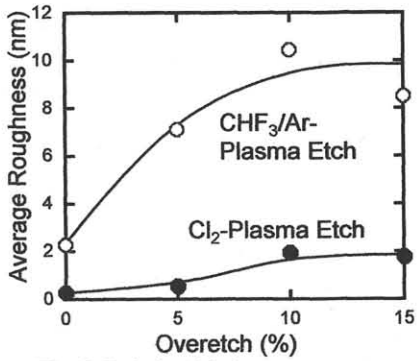

Fig. 2. Relationship between average surface roughness and overetching degree in sidewall etch-back.

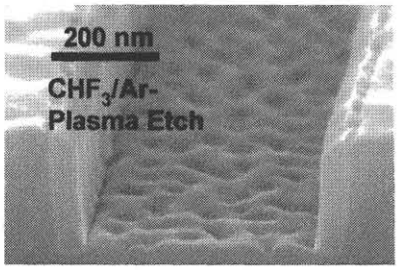

Fig. 3. SEM image of a PFET formed by CHF_3/Ar etching.

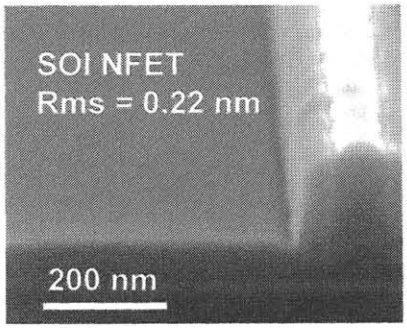

Fig. 4. SEM image of an SOI NFET with 38-nm-thick epitaxial Si.

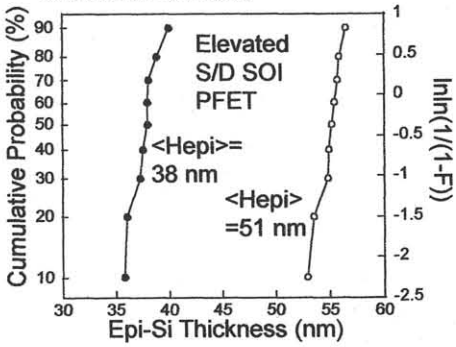

Fig. 5. Cumulative probability of epitaxial Si thickness on SOI PFETs for a mean thickness of 38 and 51 nm.

Table I. Coverage of impurities at epi-Si/sub-Si interface. 100% means one monolayer.

Sample	C	Cl	F	O
Cl_2 Etch	1.9%	0.0%	0.0%	0.3%
CHF_3/Ar Etch	118.3%	4.4%	4.5%	0.6%

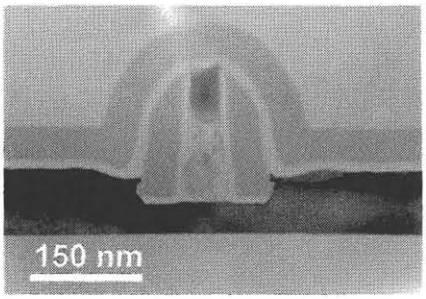

Fig. 6. TEM image of an SOI PFET with 51-nm-thick epitaxial Si.

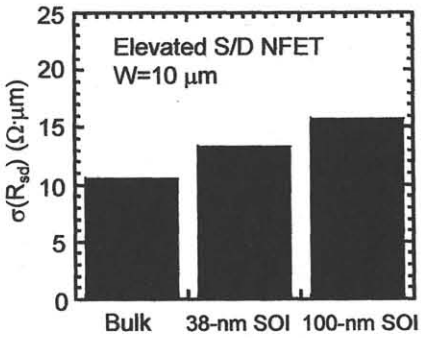

Fig. 7. Standard deviation of parasitic S/D resistance in elevated S/D NFETs with bulk, 38-nm-thick SOI, and 100-nm-thick SOI structures.

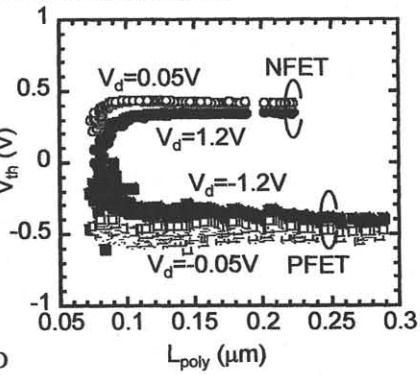

Fig. 8. Threshold voltage versus gate length for 38-nm-thick SOI N/PFETs.

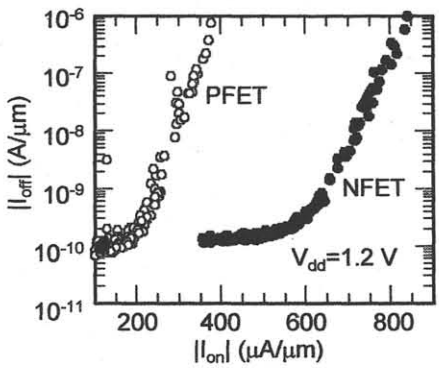

Fig. 9. I_{on}-I_{off} characteristics of 38-nm-thick SOI N/PFETs at 1.2 V.

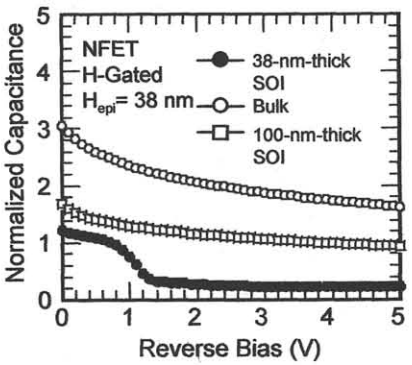

Fig. 10. Normalized junction capacitance versus reverse voltage for 38-nm-thick elevated S/D NFETs.

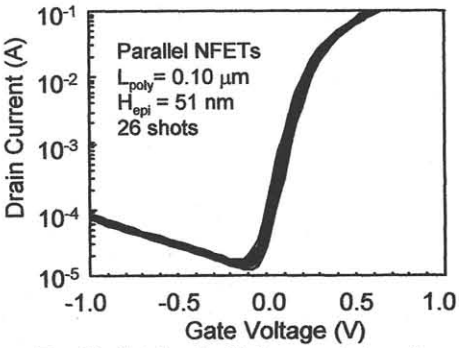

Fig. 11. Subthreshold characteristics of parallel NFETs consisting of 10,000 FETs at L_{poly} = 0.1 μm for all shots.