Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 76-77

D-1-5

Notable Advantages of High Performance SOI Technology beyond 90nm Generation

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1. Introduction

Silicon-on-insulator (SOI) technology has emerged for low power and high performance applications [1-5]. However, the floating body effect (FBE) of SOI transistor is still remained problems to be solved for highly stable circuit operation. The body contact (BC) technology eliminates the FBE. But, the body contact has an area penalty and a speed delay [2,3]. The circuit instability, layout handicap, and the performance degradation of the SOI technology give SOI chipmakers and designers mental anguish over the possibility of SOI as a mainstream technology beyond 90nm. There are little reports on advantages of the high performance SOI technology beyond 90nm technology generation. In this paper, from 250nm to 90nm technology generation, FBE, transistor performance, and SOI thickness issues are investigated. The notable advantages of the SOI technology beyond 90nm node are proposed.

2. Experimental

Body floating and body contacted SOI CMOS transistors are fabricated on SOI wafer with SOI thickness range of 70nm to 160nm. The body floating (BF) and body contact SOI transistors with 250nm, 150nm, and 90nm node technology based on Table 1 were fabricated to compare the electrical characteristics each other. As shown in Fig. 1, thin nitrided thin gate oxide was formed on the SOI layers with STI and cobalt SALICIDE process is applied.

3. Results and Discussion

Figure 2 shows threshold voltage vs. gate length for BF and BC NMOS and PMOS SOI transistors with 90nm technology. Figure 3 shows Ioff vs. Ion characteristics of BF and BC NMOS and PMOS SOI transistors with the various technology generations. For 250nm technology node, BC SOI transistors have better performance compared to BF SOI shown in Fig. 3 (a). Especially, NMOS has larger difference than PMOS, which is due to the higher Ioff value by the parasitic bipolar effect [2]. For 150nm node, the performance difference between BF and BC SOI decreases (Fig. 3 (b)). On the other hand, there is no performance difference between BF and BC SOI transistors in Ioff region higher than 5nA/μm (Fig. 3 (c)). As the technology has been scaling down from 250nm beyond 90nm, the operation voltage and off current specifications have decreased and increased, respectively (Table 1). The Ioff hump characteristics in intermediate channel length region shown in Fig. 4 is occurred due to combined effect of the parasitic bipolar effect and the reverse short channel effect in threshold voltage [2]. For BF NMOS SOI transistors, the Ioff level of 90nm technology node is much lower than that of 250nm technology node due to the reduced operation voltage. But, for BC NMOS transistors, Ioff level of 90nm technology node are slightly higher than that of 250nm technology node due to the reduced threshold voltage specification. Consequently, the difference of Ioff values between BF and BC SOI transistors is remarkably reduced in 90nm technology node, compared to 250nm node. As shown in Fig. 5, dynamic leakage current by the FBE in pass gate transistor with BF SOI is negligible at operation voltage less than 1.5V. Therefore, for low voltage application beyond 90nm technology less than 1.0V, BF SOI technology should be used sufficiently to maximize the intrinsic SOI advantages over the bulk-Si. In addition, in order to stabilize the SOI circuits, it is necessary to use the BC SOI transistors in only high voltage circuit such as I/O and analog circuit higher than 1.5V. The transistor gate delay time vs. technology generation for BF and BC SOI transistors are summarized in Fig. 6. As the technology is shrunk from 250nm to 90nm, performance difference of the BF and BC SOI transistors is negligible due to the reduced operation voltage and increased Ioff specifications shown in Fig. 6 and Table 1.

Figure 7 shows drain-induced barrier lowering (DIBL) of the 90nm node BF NMOS SOI with SOI thickness. Inset is Ids vs. Vgs characteristics for the 90nm BF NMOS SOI. For 70nm thick SOI transistor, the smallest DIBL due to the reduced FBE was observed to be 55mV. As shown in Fig. 8, the junction capacitance decreases with the SOI thickness decreasing. The 160nm thick NMOS SOI has a capacitance hump at lower voltage regime less than 1.0V, and the capacitance decreases abruptly at higher than 1.0V. That is due to the bottom junction reaching through the buried oxide layer. The sidewall junction area decreases with the SOI thickness decreasing. It leads to the reduction of the total junction capacitance (=area junction + perimeter junction) [5]. Figure 9 shows measured ring oscillator speed vs. normalized Ion for the 90nm technology node BF SOI transistors with several SOI thicknesses. Ring oscillator speed is improved up to 45% for the SOI transistors for sub-100nm thick SOI layer due to the reduced junction capacitance.

4. Conclusions

Notable advantages of high performance body floating SOI transistors beyond 90nm technology generation have been investigated. Beyond 90nm technology node, because of the reduced operation voltage and the increased Ioff specifications, the transistor performance of the body floating SOI transistor is the same as that of the body contact SOI. In addition, floating body effect in the SOI transistor is drastically suppressed due to the reduced operation voltage. So, the FBE is not critical problems any more for stable low voltage (<1.0V) and high performance circuit operation beyond 90nm technology node. Downscaling of SOI thickness beyond 90nm node gives the speed improvement up to 45% due to reduced junction capacitance as well as suppression of the FBE.

References

[1] Y. W. Kim *et al.*, *Proc. of IEEE ISSCC*, pp. 432, 1999.
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[3] H. S. Kang *et al.*, *2001 SSDM Tech. Dig.*, pp. 260, 2001.
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[5] R. Chau *et al.*, *IEEE IEDM Tech. Dig.*, pp. 621, 2001.

Table 1 High performance logic technology requirement (ITRS 1999/2000/2001.)

Generation	*250nm	150nm	90nm	65nm
Vdd [V]	*2.0	1.5	1.0	0.7
Ioff [nA/um]	*1	5 -10	100	1000
Tox [nm]	*~3.2	1.9	< 1.4	< 1.1
Tsoi [nm]	< 200	< 200	< 93	< 63

Tox : equivalent oxide thickness (EOT)
Tsoi : SOI thickness (partially depleted)
* : Intel 2.0V 0.25μm technology target

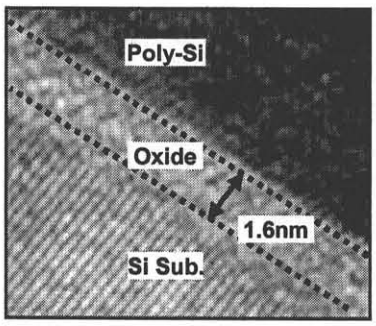


Fig. 1 TEM images for physically 1.6nm thick thin nitrided gate oxide of 90nm technology node SOI transistor **(EOT=1.4nm)**

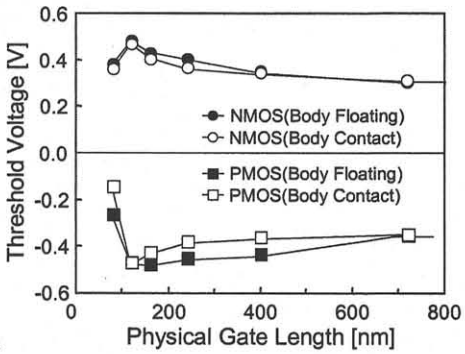
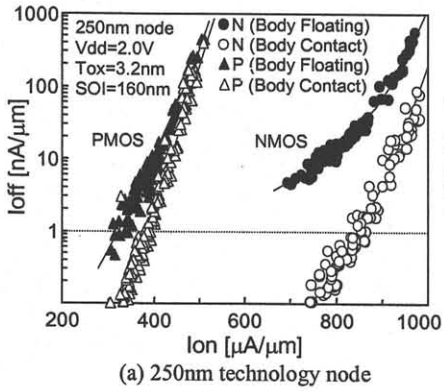
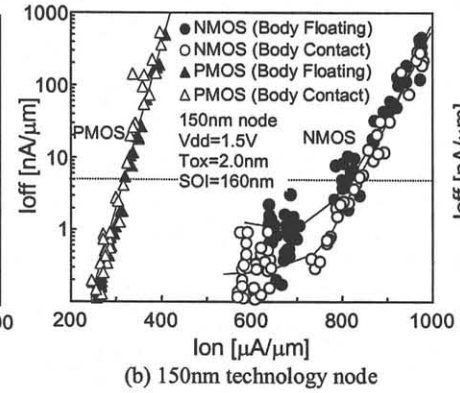


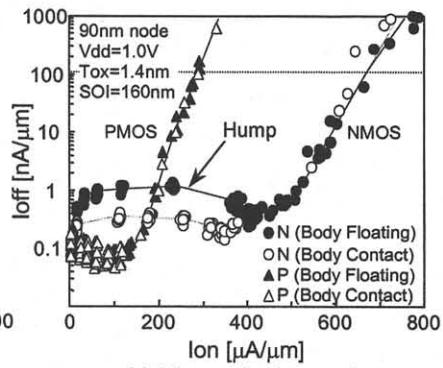
Fig. 2 Threshold voltage vs. gate length of body floating and body contacted SOI transistors at 90nm technology node.



(a) 250nm technology node



(b) 150nm technology node



(c) 90nm technology node

Fig. 3 Off current vs. drive current of body floating and body contacted NMOS and PMOS SOI transistors for technology node.

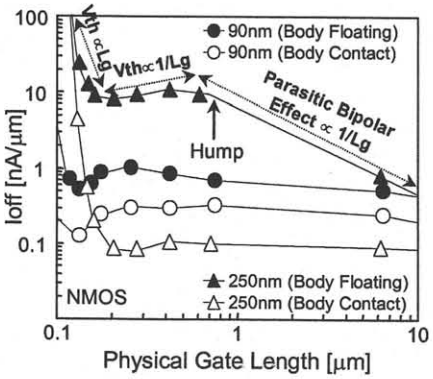


Fig. 4 Off current vs. physical gate length of 160nm thick NMOS SOI transistors at 90nm and 250nm technology nodes.

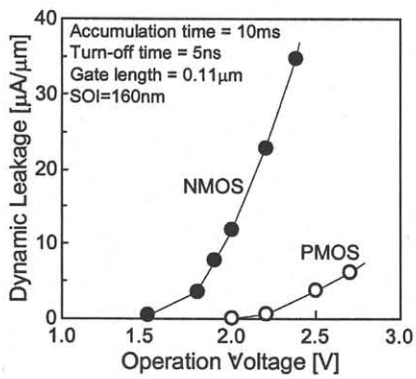


Fig. 5 Dynamic leakage current of body floating NMOS and PMOS SOI transistors with operation voltages.

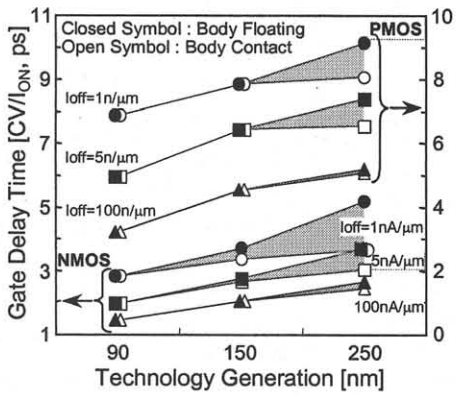


Fig. 6 Gate delay time vs. technology generation node for body floating and body contacted NMOS and PMOS SOI transistors.

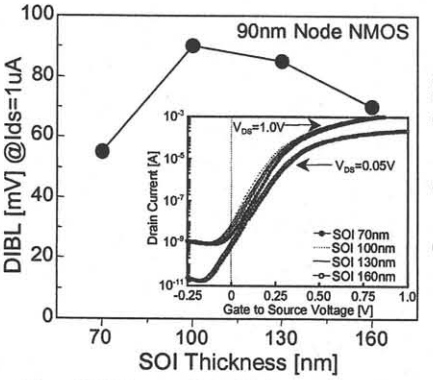


Fig. 7 DIBL vs. SOI thickness for 90nm technology node NMOS SOI transistors with gate length 0.25μm.

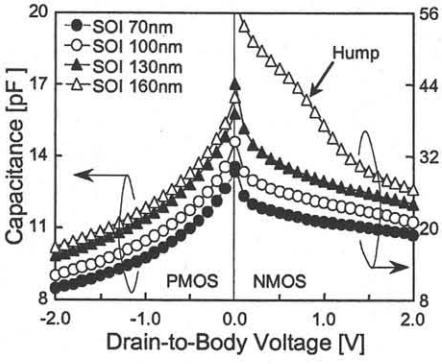


Fig. 8 Junction capacitance of 90nm technology node NMOS and PMOS SOI transistors with SOI thickness.

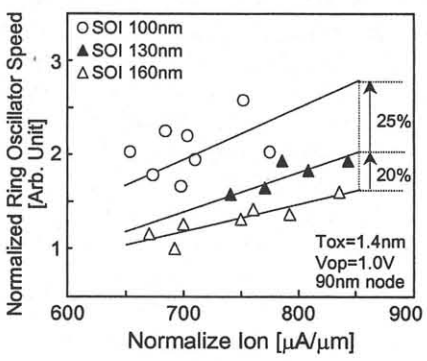


Fig. 9 Normalized ring oscillator speed vs. normalized Ion $[(NI_{ON}+2*PI_{ON})/2]$ with SOI thickness.