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High-Performance 1T1MTJ MRAM Technology with an Amorphous MTJ Material

M. Motoyoshi[1], K. Moriyama[2], H. Mori[2], C. Fukumoto[2], H. Itoh[3], H. Kano[4], K. Bessho[4], H. Narisawa[4]
1) Technology Development Group, SNC, Sony Corporation,
2) LSI Design Division, Sony Semiconductor Kyushu, 3) MOS Production Division, Sony Semiconductor Kyushu,
4) Group No. 2, Storage Technology Laboratories, Sony Corporation
4-14-1 Asahi-cho, Atsugi-shi, Kanagawa, 243-0014 Japan
Phone: +81-46-230-5662, Fax: +81-46-230-6374, E-mail: Makoto.Motoyoshi@jp.sony.com

1. Introduction

Magnetoresistive random access memory (MRAM) is a candidate to become the main form of non-volatile memory, and is likely to enable new applications such as, non-volatile logic devices. This is because of MRAM's high-speed random access, unlimited read/write endurance [1, 2], and high degree of CMOS process compatibility. The cost-competitiveness and non-volatility of MRAM even raise the possibility that it will replace DRAM and SRAM, except in ultra-fast applications. To achieve practical high-density MRAM, though, we must minimize variation in the parameters that determine memory operation across the die, wafer, and wafer batch. Another issue is how we can reduce the relatively high write current since this restricts its low-power SoC application. In this paper, we show that the MRAM read/write characteristics are improved by introducing an amorphous ferromagnetic material as a free layer of magnetic tunnel junctions (MTJs) [3]. We also explain how power dissipation during the write cycle can be reduced.

2. Experiments

The 0.4 x 0.8 um^2 MTJ elements were integrated with 0.35-um CMOS technology (Fig. 1). To start with, the CMOS circuitry and three levels of aluminum metal were formed. The interlayer on which the MTJ cells were to be placed was planarized by CMP. The MTJ material stack was then sputter deposited. Plating Cu was used to form a fourth level of metal. (Figure 2 shows cross-sectional SEM and TEM images of the MRAM cell.) The test chip consisted of three types of memory block: an 8-kbit cell array equipped with cell transistors and decoder circuits for the short pulse writing experiment; a 625 (25 x 25) -bit cell array with cell transistors to obtain the DC parameters of each bit; and individual MTJ cells without cell transistors.

3. Results and discussion

A high magnetoresistance (MR) ratio is needed for fast operation, and very tight control of MTJ resistance within the die is important for stable read-operation. Figure 3 shows the MR ratio dependence on the MTJ bias voltage. The MR ratio was 55% at 50 mV and more than 40% at 300 mV. This represents the best performance yet reported for an MTJ material. Figure 4 shows the simulated address access time of two MR devices. For a 1-Mbit MRAM, improving the MR ratio by 20% reduced delay time by 17%. The variation in both the resistance and the MR ratio across the 13 x 13 mm die was controlled to within 3%. Figure 5 is a histogram of the bit-reading resistance for 625-bit cell arrays. The MTJ with an amorphous material (CoFeB) provided better separation between '0' and '1' than that with the conventional material (CoFe). Figure 6 shows asteroid curves for conventional and amorphous MTJ materials. The curves for 80 individual MTJ cells in a die were superimposed to obtain each graph. The measurement was done with the two-axis-variable magnetic fields induced by magnetic coils. The conventional material provided no single operating point. All asteroid curves for CoFeB were, however, much more similar to each other and thus provided an obvious operating point. Figure 7 shows the writing yield of 625-bit cell array obtained when we used an LSI tester to measure it. There seems to be a strong correlation between the switching magnetic field from 80 cells and switching current from the 625-bit cell array. When the measured switching current of the 625-bit cell array was used, the switching magnetic field obtained from single-cell measurement was in good agreement with the simulation result. One ways to improve power consumption in MRAM writing cycle is to shorten the writing pulse. Figure 8 shows the relationship between the failure rate and pulse duration. Writing operation with a 2.5-ns write-pulse width was achieved. Decreasing the write pulse current increased the failure rate and the difference between the witching current of for '1' and for '0' became larger (Fig. 9). This suggests greater asymmetry of the asteroid curves in the case of short pulse writing. Thus, care in optimizing the shape of the MTJ cells and reducing Hfis necessary for a short-pulse writing operation. Increasing the magnetic field by reducing the gap between the write word line and the MTJ is one way to reduce the writing current. Figure 10 shows the dependence of the magnetic field efficiency on the gap based on simulation results. Reducing the gap from 400 nm to 100 nm halves the writing current required in the write word line. Short pulse writing combined with a narrow gap structure should allow us to reduce the cell-array power consumption to the DRAM level (Fig. 11).

4. Conclusion

We successfully integrated 0.4 x 0.8 um^2 MTJ elements with 0.35-um CMOS technology without device degradation. An MR ratio of more than 55% and an optimum read/write operating point were obtained by introducing an improved MTJ material. But designing high density MRAM, it is necessary the further improvement of the uniformity of the switching magnetic field. The effects of short-pulse writing combined with an improved cell structure suggest that MRAM is promising for low power applications.

Acknowledgment

We thank H. Tsukazaki, N. Okazaki, and K. Hayashi for their support of this work.

References

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[2] M. Durlam, et al., "Nonvolatile RAM based on Magnetic Tunnel Junction Elements," ISSCC Dig. Tech. Papers, pp. 130-131, Feb. 2000

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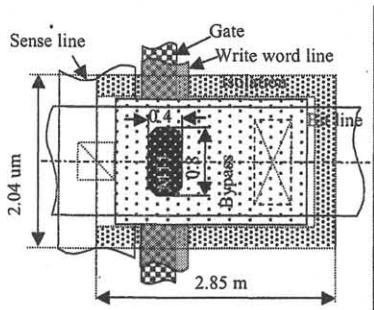

Fig. 1 Layout of the 0.35-um cell

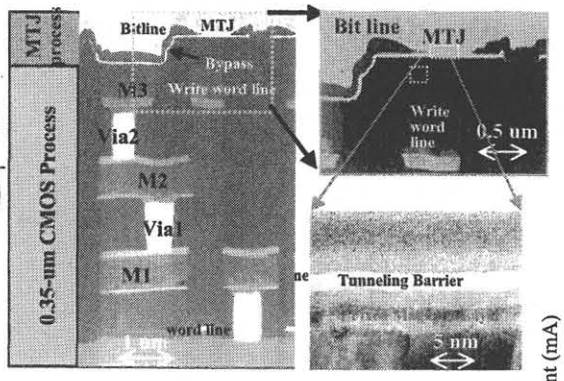

Fig. 2 Cross-sectional images of MRAM

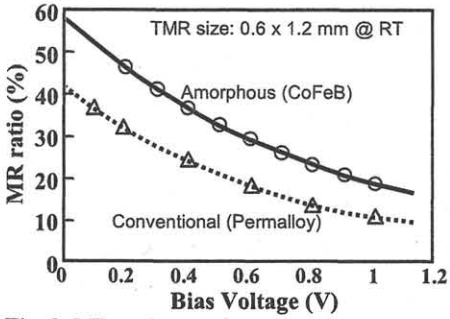

Fig. 3 MR ratio as a function of bias voltage

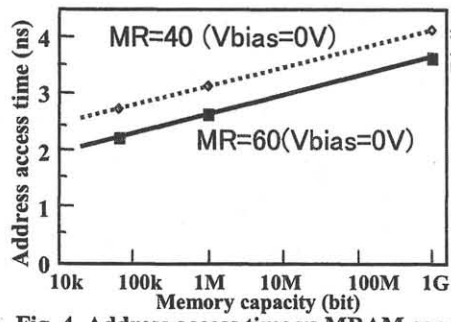

Fig. 4 Address access time vs MRAM capacity

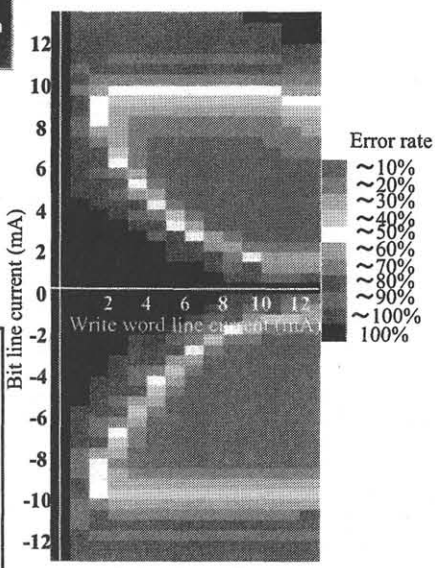

Fig. 7 Writing yield of 625-bit cells

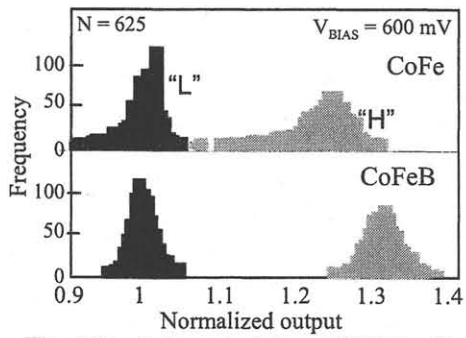

Fig. 5 Read characteristics of 625-bit cell arrays

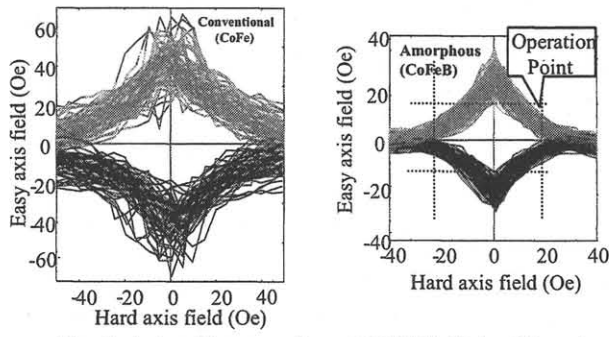

Fig. 6 Asteroid curves from 80 MTJs (0.4 x 0.8 um)

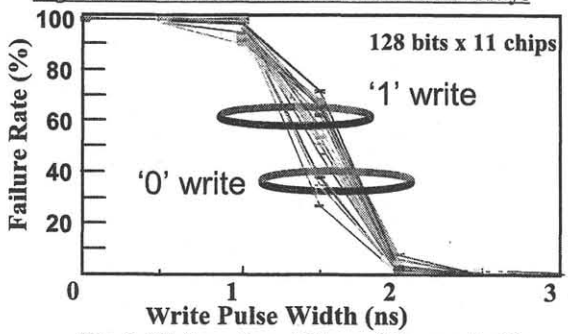

Fig. 8 Write pulse width vs. failure rate (1)

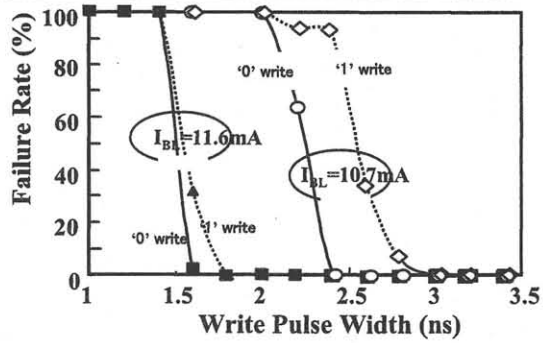

Fig. 9 Write pulse width vs. failure rate (2)

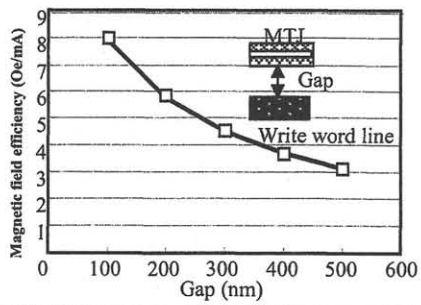

Fig. 10 Induced magnetic field of write word line (simulation)

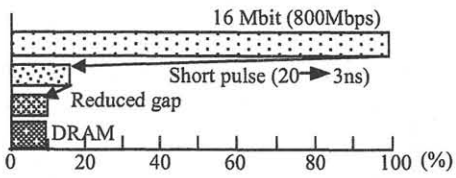

Fig. 11 Comparison of power consumption between 16-Mbit MRAM and DRAM cell arrays