

## D-2-2 (Invited)

## The Issues and Reliability of High Density FeRAMs

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**F**erroelectric **R**andom **A**ccess **M**emory (FeRAM) is one of the strong candidates for application in mobile electronic devices, such as smart card, cellular phone and PDA, due to low operation voltage, fast write speed, and high read/write endurance with non-volatility. For the realization of high density commercial FeRAMs, some technical issues should be resolved clearly. Due to the reliability concerns of ferroelectric materials, such as fatigue, retention, and imprint, it isn't easy to obtain the scaled FeRAM cells. Fig. 1 shows cell signal distributions and changes due to imprint degradation after high temperature storage. The extra-sensing margin considering the imprint degradation is an important factor that increases a cell size. In order to overcome the drawback, we have to make effective efforts for the improvements of ferroelectric capacitor module process and design architecture. The fatigue and imprint degradation of ferroelectric capacitor are significantly suppressed by

the newly developed  $(\text{Bi}_{1-x}\text{La}_x)_4\text{Ti}_3\text{O}_{12}$  (BLT) films. The key process is a crystallization control by special bake treatments to obtain high polarization at low temperatures less than  $650^\circ\text{C}$ . The advanced design architectures, such as split word line (SWL) cell array and current gain cell (CGC) operation scheme show a high device performance and cell efficiency. In SWL, the larger size of cell array block can be achieved by merging a word line (WL) and its neighboring plate line (PL). The SWL array merges two conventional 1T1C cell array block into one SWL array with open-bit line (BL) as shown in Fig. 2. The CGC operation has high sensing margin with optimized sub-bit line capacitance ( $<100\text{ fF}$ ), high cell efficiency, and small cross-talk noise. By using the above design architectures, the chip size can be reduced down to 63%.

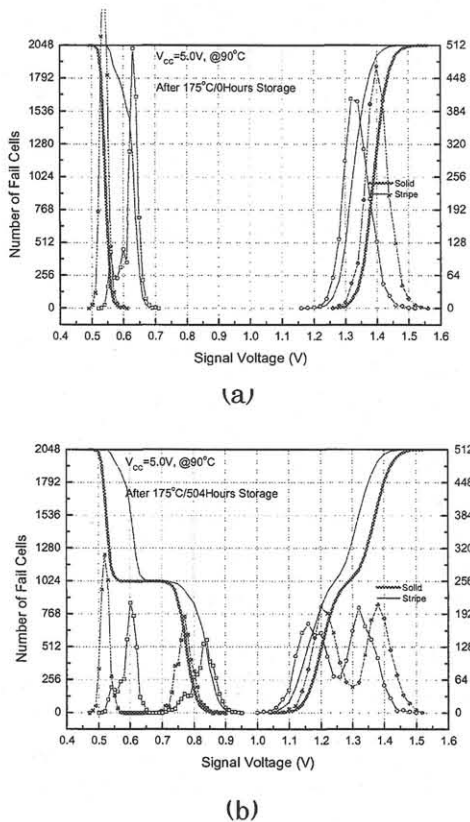


Fig. 1 Cell signal distributions (a) before and (b) after storage at

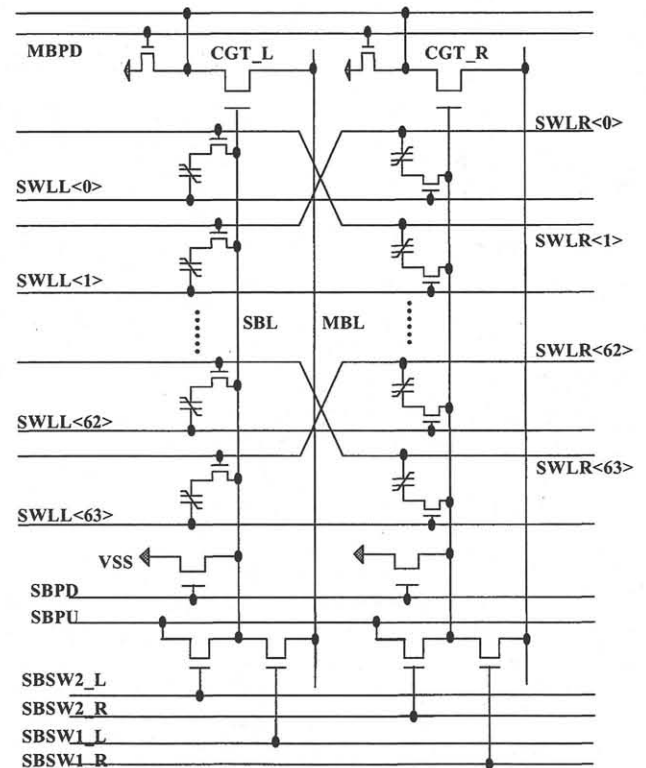


Fig. 2 The circuit diagram of SWL and CGC operation scheme

